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⑦① Applicant: **SHARP KABUSHIKI KAISHA**
22-22 Nagaike-cho
Abeno-ku
Osaka 545 (JP)

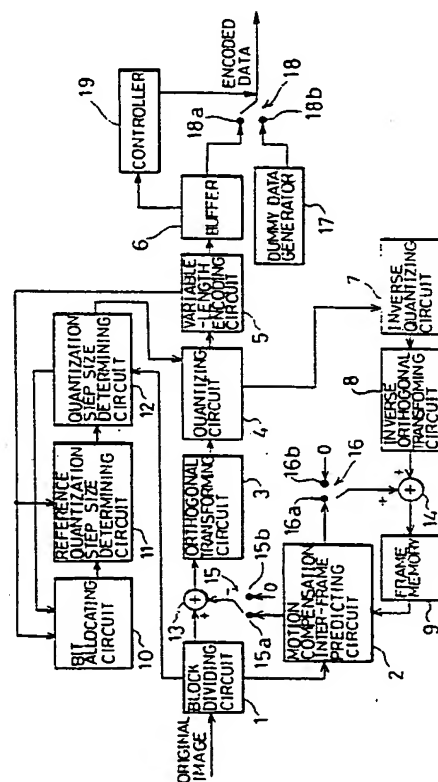
⑦② Inventor: **Katata, Hiroyuki**
2506-1-G101
Goi Ichihara-shi, Chiba 290 (JP)
Inventor: **Kusao, Hiroshi**
1716-4-B2, Toke-cho,
Midori-ku
Chiba-shi, Chiba 267 (JP)
Inventor: **Fujiwara, Yohichi**
2876-11-216, Kamatori,
Midori-ku
Chiba-shi, Chiba 266 (JP)

⑦④ Representative: **Brown, Kenneth Richard et al**
R.G.C. Jenkins & Co.
26 Caxton Street
London SW1H 0RJ (GB)

⑤④ Image encoding apparatus.

⑤⑦ In an image encoding apparatus, image information is quantized and variable-length encoding is performed thereon so that the data are stored in a buffer. Thereafter, the data in the buffer are transmitted to the outside at a fixed data rate. At this time, a controller monitors a number of occupied bits in the buffer, and when the number of occupied bits is not more than thresholds, the controller switches the output of the apparatus to a dummy data generator. At this time, a parameter which is used for rate control is initialized, and dummy data which can be eliminated on a decoding circuit are outputted from the dummy data generator. Furthermore, bit allocation is changed so that a sum of the number of occupied bits and the bit allocation to a frame which is determined before encoding does not exceed a fixed amount. Moreover, when the number of occupied bits exceeds the fixed value, a quantization step size is changed to a greater value. This efficiently prevents underflow and overflow of the buffer, and the image information can be encoded with excellent quality.

FIG. 1



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FIELD OF THE INVENTION

The present invention relates to an image encoding apparatus which is provided to an apparatus for performing a digital image process, such as a videophone, a digital video disk apparatus, and which encodes image information efficiently in order to improve efficiency of recording and transmitting of image information.

BACKGROUND OF THE INVENTION

In the case where image information with a wide band is recorded or transmitted, if the image information have its original configuration, a capacity of a recording medium and a transmitting medium is required for an amount of its data amount, so efficiency of recording and transmitting is deteriorated. For this reason, an amount of data of image information is generally compressed so as to be suitable for an ability in recording of a recording medium or an ability in transmitting of a transmitting medium. Such a data compressing process is realized by encoding high-efficiently digital motion picture information by means of arts, such as motion compensation inter-frame prediction, orthogonal transformation, quantization, variable-length encoding.

For example, in a high-efficient encoding system cited in the literature "MPEG2 Interframe Prediction" (the Institute of Television Engineers, Technical Report Vol. 16 No. 61. pp. 37-42), there exist a frame on which only intra-frame encoding is performed (hereinafter, referred to as I picture), a frame on which predictive encoding from the previous frame is performed (hereinafter, referred to as P picture) and a frame on which predictive encoding from the previous and subsequent frames is performed (hereinafter, referred to as B picture). An amount of codes generated in I picture is great, an amount of codes generated in P picture is smaller than that in the I picture, and an amount of codes generated in B picture is fairly smaller than those in the I picture and the P picture.

When the high efficient encoding system is applied to image transmission and image storing (recording), there arises a problem how a data rate after encoding (hereinafter, referred to as encoded data) is controlled.

For example, the literature "MPEG2 Quantization and Coding Control" (the Institute of Television Engineers, Technical Report Vol. 16 No. 61. pp. 43-48) discloses a method for almost constantly controlling an average number of bits in a given interval which is called group of pictures (hereinafter, referred to as GOP) (an interval from I picture to next I picture, and a number of pictures in the GOP is normally ten-odd frames).

Fig. 16 is a block diagram of an image encoding apparatus utilizing a conventional method.

First, in a block dividing circuit 51, a frame to be encoded is divided into blocks which are called a macroblock (hereinafter, referred to as MB). Intra-frame encoding or inter-frame encoding is performed per MB.

In a motion compensation inter-frame predicting circuit 52, a current frame is compared with a frame previously encoded and decoded so that while an amount of a move of MB (move vector) is being detected, the MB is predicted from a decoded frame. However, MB of I picture and MB in which intra-frame encoding is advantageous are not predicted. The predicting method is disclosed in the literature "MPEG2 Interframe Prediction" (the Institute of Television Engineers, Technical Report Vol. 16 No. 61. pp. 37-42).

In an orthogonal transforming circuit 53, the data of MB are transformed to data suitable for encoding by two-dimensional orthogonal transformation (for example, discrete Fourier transformation, Hadamard transformation, discrete cosine transformation, etc.). At this time, in the case of intra-frame encoding, two-dimensional orthogonal transformation is carried out on the data of MB from the block dividing circuit 51, whereas in the case of inter-frame encoding, a switch 54 is switched to the motion compensation inter-frame predicting circuit 52, a prediction difference (prediction error) is obtained by a subtracter 55 and two-dimensionally orthogonal transformation is carried out on the prediction error.

In a quantizing circuit 56, transform coefficients are quantized by a quantization step size obtained in a quantization step size determining circuit 66, and in a variable-length encoding circuit 57, variable-length encoding is performed on the quantized transform coefficient. Then, in a buffer 58, the output from the variable-length encoding circuit 57 is temporarily stored and encoded data are outputted at a determined constant data rate.

In addition, the transform coefficient quantized in the quantizing circuit 56 are inversely quantized in an inverse quantizing circuit 59 and inverse orthogonal transformation is carried out on inversely quantized transform coefficient in an inverse orthogonal transform circuit 60.

In the case of inter-frame encoding, since the reconstructed value from the inverse orthogonal transforming circuit 60 is the data of the prediction difference, a switch 62 is switched to a terminal 62a side, and in an adder 61, the data of the prediction difference as the reconstructed value and prediction MB outputted from the motion compensation inter-frame predicting circuit 52 are added so that reconstructed image data can be obtained. Meanwhile, in the case where the reconstructed value from the inverse orthogonal transforming circuit 60 is the data of MB on which intra-frame encoding is performed, since the reconstructed data directly becomes reconstructed image data, the switch 62 is switched to a terminal

62b side.

The reconstructed image data are stored in a frame memory 63. The reconstructed image data are used as a reference image for inter-frame prediction in the motion compensation inter-frame predicting circuit 52.

In addition, in the conventional image encoding apparatus, encoding control is performed by a bit allocating circuit 64, a reference quantization step size determining circuit 65 and a quantization step size determining circuit 66. The following will discuss the encoding control in detail.

The bit allocating circuit 64 determines a number of bits which are allocated to a frame to be encoded per frame based upon the encoded results up to the previous frame (a number of generated bits obtained from the various-length encoding circuit 57, and an average value of quantization widths obtained from the quantization step size determining circuit 66) and the given data rate. Concretely, global complexity measures X_I , X_P and X_B of I picture, P picture and B picture are determined according to the following formulas (1) through (3).

$$X_I = S_I \bar{Q}_I \quad (1)$$

$$X_P = S_P \bar{Q}_P \quad (2)$$

$$X_B = S_B \bar{Q}_B \quad (3)$$

In the formulas (1) through (3), S_I , S_P and S_B represent an amount of encoded data of previous I picture, P picture and B picture (a number of generated bits). Moreover, \bar{Q}_I , \bar{Q}_P and \bar{Q}_B represent an average quantization step size at the time of encoding of previous I picture, P picture and B picture.

The global complexity measures are based upon that when an image to be encoded is complex, a number of generated bits increase and a quantization step size tends to be enlarged in order to restrict increase in the number of generated bits. However, a fixed initial value is set as the global complexity measures at the beginning of encoding.

Next, as to the bit allocating circuit 64 determines target bit allocation T_I , T_P and T_B to an image to be encoded of I picture, P picture and B picture according to calculation of the following formulas (4) through (6).

$$T_I = \frac{R}{1 + \frac{N_P X_P}{K_P X_I} + \frac{N_B X_B}{K_B X_I}} \quad (4)$$

$$T_P = \frac{R}{N_P + \frac{N_B K_P X_B}{K_B X_P}} \quad (5)$$

$$T_B = \frac{R}{N_B + \frac{N_P K_B X_P}{K_P X_B}} \quad (6)$$

In the above formulas (4) through (6), R represents a number of remained bits in GOP, N_P and N_B represent a number of P pictures and B pictures which have not been encoded yet in GOP, and K_P and K_B represent constants.

Next, the reference quantization step size determining circuit 65 and the quantization step size determining circuit 66 determine a quantization step size by using the values T_I , T_P and T_B . In the case of I pictures, in order to obtain a quantization step size, a reference quantization step size q_I^j which becomes a basis is first obtained and is compensated according to an activity of an image so that a quantization step size Q_I^j (j is a number of MB) is obtained. Also as to P picture and B picture, since a quantization step size can be determined in the same manner as of I picture, the following will discuss determination of a quantization step size of I picture.

First, in the reference quantization step size determining circuit 65, a reference quantization step size of orthogonal transformation coefficient is determined per MC based upon a number of generated bits up to the previous MB obtained in the variable-length encoding circuit 57 and a number of bits T_I which is allocated by the bit allocating circuit 64.

In other words, the reference quantization step size determining circuit 65 determines virtual buffer fullness d_I^j in the j -th block of I picture according to the following formula (7).

$$d_I^j = d_0^I + B_I - 1 - \frac{T_I(j-1)}{MBcnt} \quad (7)$$

The reference quantization step size determining circuit 65 determines a reference quantization step size q_I^j per MC according to calculation of the following formula (8).

$$q_I^j = \frac{31d_I^j}{r} \quad (8)$$

In the formula (7), d_0^I is an initial buffer fullness (final buffer fullness q MBcnt I at the time of encoding previous I picture, and its initial value is a certain constant), B_I is a total number of bits generated in an image up to the j -th block, and MBcnt is a total number of MB in an image. Furthermore, r in the formula (8) is a constant which is called a reaction parameter.

In the formula (7), T_I bit is equally allocated to each MB, and a difference between a number of allocated bits up to the previous MB and a number of actually generated bits is reflected in the virtual buffer fullness. Therefore, if a number of generated bits up to the previous MB is great, the virtual buffer fullness becomes large, and also the reference quantization step size becomes large, so a number of subsequently generated bits is restricted. On the contrary, if the number of generated bits up to the previous MB is small, the virtual buffer fullness becomes small, and also the reference quantization step size becomes small, so a number of subsequently generated bits is enlarged. Here, in P picture and B picture, reference quantization widths q_I^P and q_I^B are determined in the same manner.

In the quantization step size determining circuit 66, an activity which shows fineness of a picture in

MB obtained from the block dividing circuit 51 is calculated per MB, and the reference quantization step size q_j^1 is changed by the activity per MB so that a quantization step size which is used in the quantizing circuit 56 is determined.

In other words, the quantization step size determining circuit 66 determines the quantization step size Q_j^1 of the j -th MB in I picture is determined according to the following formula (9).

$$Q_j^1 = q_j^1 Nact_j \quad (9)$$

Here, $Nact_j$ in the formula (9) is an activity of the j -th MB which is normalized, and it is represented by the following formula (10).

$$Nact_j = \frac{2act_j + avg}{act_j + 2avg} \quad (10)$$

In the formula (10), act_j is the activity of the j -th MB, and avg is an average value of the activities in a previously encoded frame (it is not always I picture) (however, a predetermined initial value is set for activity at the beginning of encoding). Here, also in P picture and B picture, quantization widths Q_j^P and Q_j^B are determined in the same manner as in the above.

In order to explain the problem of the conventional image encoding apparatus, the following will discuss a number of occupied bits in the buffer 58 in the image encoding apparatus (different from the virtual buffer fullness mentioned in the prior arts).

Here, the occupied bits in the buffer 58 is defined as follows. In other words, in the case where after encoding of each image frame and storing of encoded data in the buffer 58 are instantly completed in an image encoding apparatus, the encoded data are outputted at a constant data rate, buffer occupied bits are defined as a number of bits of the encoded data which remain in the buffer 58.

Fig. 17 shows an example of an aged change in the number of occupied bits in the buffer 58 with respect to a typical motion picture sequence (image 1). Here, a horizontal axis shows a time which is represented by a frame, a vertical axis shows the number of occupied bits in the buffer 58, and an initial number of occupied bits is 0. Moreover, a bit rate is 6 Mbps, a number of frames in GOP is 15, and an interval between I picture and P picture and an interval between P pictures are 3 frames.

As is clear from Fig. 17, at time 0 a lot of data are generated by encoding I picture, but as to subsequent P picture and B picture, an encoding amount is adjusted, so the number of occupied bits in the buffer 58 substantially returns to the initial value with respect to first images in each GOP (time 15, 30, 45, etc.). In this manner, if data amount control in the GOP is satisfactorily made, the first number of occupied bits in the buffer 58 in each GOP always returns to near the initial value. Therefore, it is sufficient that a capacity of the buffer 58 is 10^6 bit, for example.

The following will discuss a motion picture se-

quence including stop motion or frequent scene changes. In a sequence which is shifted to a normal motion picture after stop motion continues for 30 frames (image 2), a number of occupied bits in the buffer 58 is shown by a solid line in Fig. 18. In a sequence which is shifted to a normal motion picture after frequent scene changes continue for 30 frames (image 3), a number of occupied bits in the buffer 58 is shown by a broken line in Fig. 18.

In the case where the capacity of the buffer 58 is 10^6 bit, as shown in fig. 18, data overflow greatly after time 15 and after time 30 in the image 2, that is, overflow occurs. The overflow occurs after time 15 of the image 2, for when a new GOP starts in a stop motion and I picture appears, extraordinarily many number of bits are allocated to the I picture and a lot of encoded data is generated. Moreover, also in I picture in a motion picture immediately after the stop motion, a lot of encoded data is generated, so overflow occurs even after time 30 in the image 2.

In order to avoid such overflow, the capacity of the buffer 58 should be enlarged, but this arises a problem that a scale of hardware increases. Moreover, in the case where a lot of encoded data is generated partially (all at once) compared to the above-mentioned normal sequence, a remaining number of bits allocated to GOP (a number of remaining bits in GOP) is extremely decreased. Therefore, there arises a problem that quality of an image thereafter is remarkably deteriorated.

In addition, there exist no encoded data in the buffer 58 after time 53 of the image 2, at times 25 through 29 of the image 3, etc., so underflow occurs. This can be a problem in actual hardware. Moreover, in the case where underflow occurs, a rate is not successively controlled, so there arises a problem that quality of an image is remarkably deteriorated due to encoding by using an inappropriate quantization step size.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide an image encoding apparatus which is capable of encoding an image with good quality and without underflow of a buffer.

In order to achieve the above object, the image encoding apparatus of the present invention is characterized by including:

- (1) quantizing means for quantizing information which corresponds to an image;
- (2) variable-length encoding means for performing variable-length encoding on the quantized result of the quantizing means;
- (3) temporary storage means for temporarily storing encoded data from the variable-length encoding means so as to transmit the stored encoded data to the outside at a fixed data rate;

(4) encoded data amount control means for calculating a quantization step size for quantizing information to be encoded based upon the encoded result of the variable-length encoding means so as to control an amount of the encoded data of the variable-length encoding means;

(5) dummy data generating means for generating dummy data which can be eliminated on a decoding side for decoding the encoded data;

(6) switching means for switching an output of the image encoding apparatus to either the encoded data from the temporary storage means or to the dummy data from the dummy data generating means; and

(7) control means for monitoring a number of occupied bits in the temporary storage means so as to control a switching operation of the switching means so that the output of the image encoding apparatus becomes the encoded data from the temporary storage means when the number of occupied bits exceeds a predetermined threshold, whereas so as to suspend transmission of data in the temporary storage means and control the switching operation of the switching means so that the output of the image encoding apparatus becomes the dummy data generated from the dummy data generating means when the number of occupied bits is not more than the threshold.

With the above arrangement, the information corresponding to image information is quantized by the quantizing means and variable-length encoding is performed on the quantized result by the variable-length encoding means so that the encoded data are stored in the temporary storage means. In this case, an amount of encoded data in the variable-length encoding means is controlled by the encoded data amount control means which calculates a quantization step size of information to be encoded based upon the encoded result of the variable-length encoding means so as to adjust a quantization step size of quantization in the quantizing means according to the calculated result. The encoded data stored in the temporary storage means are transmitted to the outside at a data rate, which is suitable for a process by an outer apparatus. At this time, it is necessary to adjust a number of occupied bits in the temporary storage means (an amount of encoded data stored in the temporary storage means) so that the generated encoded data do not exceed a memory capacity of the temporary storage means (occurrence of overflow), and the encoded data to be transmitted to the outside do not run out in the temporary storage means (occurrence of underflow).

Therefore, the dummy data generating means for generating dummy data which can be eliminated on a decoding circuit for decoding the encoded data is provided so that an output of the image encoding apparatus can be switched to either the encoded data

from the temporary storage means or the dummy data from the dummy data generating means by the switching means. Furthermore, the number of occupied bits in the temporary storage means is monitored by the control means. The switching operation of the switching means is controlled by the control means so that if the number of occupied bits exceeds the predetermined thresholds, the output of the image encoding apparatus is the encoded data from the temporary storage means, and if the number of occupied bits is not more than the thresholds, the output of the image encoding apparatus is the dummy data from the dummy data generating means.

Therefore, if the number of occupied bits in the temporary storage means is not more than the thresholds, the dummy data from the dummy data generating means are outputted from the image encoding apparatus instead of the encoded data read out from the temporary storage means. While the dummy data are being outputted, the transmission of the encoded data in the temporary storage means is suspended. During this operation, if the number of occupied bits in the temporary storage means exceeds the thresholds, the encoded data in the temporary storage means are again outputted at a constant data rate. For this reason, a lower limit of the number of occupied bits in the temporary storage means can be substantially limited to the thresholds, so the underflow of the temporary storage means can be prevented.

In addition, it is preferable that when the number of occupied bits is not more than the thresholds, the control means (7) outputs a switching signal to the encoded data amount control means, and when the switching signal is inputted, the encoded data amount control means (4) controls initializes various parameters which are used for calculation of the quantization step size. As a result, even when the dummy data are outputted instead of the actual encoded data, the parameters which are used for rate control can keep their balance and the stable rate control can be made. Therefore, a deterioration in quality of an image can be restrained.

It is another object of the present invention to provide an image encoding apparatus which is capable of encoding an image without overflow in a buffer and with good quality.

In order to achieve the above object, another image encoding apparatus of the present invention having the quantization means (1), the variable-length encoding means (2) and the temporary storage means (3) is characterized by including:

(8) encoded data amount control means for calculating bit allocation per frame of information to be encoded based upon the encoded result of said variable-length encoding means and calculating a quantization step size from the above calculated result so as to control an amount of the encoded data of said variable-length encoding means by adjusting the

quantization step size of quantization in said quantizing means according to the above calculated result, wherein said encoded data amount control means (8) includes bit allocation changing means for monitoring a number of occupied bits in the temporary storage means so as to change the calculated bit allocation when the sum of bit allocation to a frame which has been calculated before encoding and a number of occupied bits in said temporary storage means at the time of the calculation of the bit allocation exceeds the predetermined thresholds, such that the sum does not exceed the thresholds.

With the above arrangement, the encoded data amount control means calculates bit allocation per frame of information to be encoded so as to determine a quantization step size. The encoded data amount control means includes bit allocation changing means for changing the calculated bit allocation. The bit allocation changing means monitors the number of occupied bits in the temporary storage means and changes the calculated bit allocation so that a sum of the bit allocation to a frame calculated before encoding and the number of occupied bits in the temporary storage means at the time of calculation of the bit allocation do not exceed the predetermined thresholds. Therefore, even when the frame information are encoded and stored in the temporary storage means, the number of occupied bits in the temporary storage means at this time do not greatly exceed the thresholds. As a result, the overflow can be prevented by setting the thresholds to smaller values than the memory capacity of the temporary storage means.

In addition, it is desirable that the encoded data amount control means (8) further includes quantization step size changing means for monitoring the number of occupied bits in the temporary storage means so as to change the calculated quantization step size to a greater value when the number of occupied bits exceeds the fixed thresholds. This makes it possible to efficiently prevent the overflow of the temporary storage means.

For a fuller understanding of the nature and advantages of the invention, reference should be made to the ensuing detailed description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram which shows an arrangement of a main circuit in an image encoding apparatus of the first embodiment of the present invention.

Fig. 2 is a graph which shows an aged change in a number of occupied bits in a buffer in the case where information corresponding to an image (image 3) which is shifted to a normal motion picture after frequent scene changes continue for 30 frames is encoded by the image encoding apparatus shown in Fig. 1.

Fig. 3 is an explanatory drawing which explains an arrangement of GOP and a inter-frame predicting method.

Fig. 4 is a block diagram which shows an arrangement of a main circuit in an image encoding apparatus of the second embodiment of the present invention.

Fig. 5 is a graph which shows an aged change in a number of occupied bits in a buffer in the case where information corresponding to the image 3 is encoded by the image encoding apparatus shown in Fig. 4.

Fig. 6 is a block diagram which shows an arrangement of a main circuit in an image encoding apparatus of the third embodiment of the present invention.

Fig. 7 is a graph which shows an aged change in a number of occupied bits in a buffer in the case where information corresponding to an image (image 2) which is shifted to a normal motion picture after stop motion continues for 30 frames is encoded by the image encoding apparatus shown in Fig. 6.

Fig. 8 is a block diagram which shows an arrangement of a main circuit in an image encoding apparatus of the fourth embodiment of the present invention.

Fig. 9 is a graph which shows a relationship between a value α , which is multiplied by a quantization step size so as to change the quantization step size used for the image encoding apparatus shown in Fig. 8, and a number of occupied bits in a buffer BO.

Fig. 10 is a graph which shows an aged change in a number of occupied bits in a buffer in the case where information corresponding to the image 2 is encoded by the image encoding apparatus shown in Fig. 8.

Fig. 11 is a block diagram which shows an arrangement of a main circuit in an image encoding apparatus including all methods in embodiments 1 through 4.

Fig. 12 is a graph which shows an aged change in a number of occupied bits in a buffer in the case where information corresponding to the image 2 and the image 3 is respectively encoded by the image encoding apparatus shown in Fig. 11.

Fig. 13 is an explanatory drawing which shows a format of dummy data generated from a dummy data generator in the image encoding apparatus shown in Fig. 1.

Fig. 14 is an explanatory drawing which shows another format of the dummy data generated from the dummy data generator in the image encoding apparatus shown in Fig. 1.

Fig. 15 is an explanatory drawing which shows still another format of the dummy data generated from the dummy data generator in the image encoding apparatus shown in Fig. 1.

Fig. 16 is a block diagram which shows an arrangement of a main circuit in a conventional image encoding apparatus.

Fig. 17 is a graph which shows an aged change

in a number of occupied bits in a buffer in the case where a typical motion picture is encoded by the image encoding apparatus.

Fig. 18 is a graph which shows an aged change in a number of occupied bits in a buffer in the case where information corresponding to the image 2 and the image 3 is respectively encoded by the conventional image encoding apparatus.

DESCRIPTION OF THE EMBODIMENTS

[EMBODIMENT 1]

The following description will discuss one embodiment of the present invention mainly referring to Figs. 1 through 3 and Figs. 13 through 15.

The image encoding apparatus of the present invention controls underflow of a buffer which is one of the problems in the prior arts, and an arrangement of its main part is shown in Fig. 1.

As shown in Fig. 1, the image encoding apparatus includes a block dividing circuit 1, a motion compensation inter-frame predicting circuit 2, an orthogonal transforming circuit 3, a quantizing circuit 4 as quantizing means, a variable-length encoding circuit 5 as variable-length encoding means, a buffer 6 as temporary storing means, an inverse quantizing circuit 7, inverse orthogonal transforming circuit 8, a frame memory 9, a bit allocating circuit 10, a reference quantization step size determining circuit 11, a quantization step size determining circuit 12, a subtracter 13, an adder 14 having two input terminals, a switch 15 for switching an input to a minus input terminal of the subtracter 13, a switch 16 for switching an input to one input terminal of the adder 14, a dummy data generator 17 as dummy data generating means, a switch 18 as switching means for switching whether an output of the image encoding apparatus is performed from the buffer 6 or the dummy data generator 17, and a controller 19 as control means for controlling the switch 18 while supervising a number of occupied bits in the buffer 6.

In the same manner as the prior arts, the image encoding apparatus divides a frame to be encoded into, for example, MBs of 16x16 pixels and intra-frame encoding or intra-frame predictive encoding is performed per MB. There exists a frame on which only intra-frame encoding is performed (I picture), a frame on which inter-frame predictive encoding is performed from previous frame (P picture), and a frame on which inter-frame predictive encoding is performed from previous and subsequent frames (B picture). The intra-frame encoding is performed at a predetermined frame interval. In the present embodiment, the intra-frame encoding is performed per 15 frames (in other words, a number of frames in GOP N is 15), but the present invention is not limited to this, so a number of frames in the GOP N can be changed

by setting.

As shown in Fig. 3, a first image (frame) in the GOP is an I picture. Non intra prediction is performed on a P picture after a predetermined number of frames M from the I picture, and from the I picture and the P picture, inter-frame prediction is performed on a B picture between the I picture and the P picture. Moreover, inter-frame prediction is performed on a P picture after a predetermined number of frames M from P picture on which inter-frame prediction has been performed from the I picture, and from the both P pictures, inter-frame prediction is performed on B picture between the P pictures. In this manner, as to P picture, inter-frame prediction is performed from previous I picture or previous P picture, and as to B picture, inter-frame prediction is made from I picture or P picture before and after the B picture. As to an arrangement of the GOP in a number of frames N, a first frame in the GOP is an I picture, $(1 + nM)$ th frame in the GOP is a P picture (however, $1 + nM \leq N$, n is a natural number), frames other than the above frames in the GOP are B pictures. In the present embodiment, as shown in Fig. 3, an interval between an I picture and a P picture and an interval between P pictures M are 3, but the present invention is not limited to this, so M may be 2 or not less than 4.

As shown in Fig. 1, an original image is inputted to the block dividing circuit 1 (after in the case where the original image is analog, it is transformed to digital), and a frame to be encoded is divided into, for example, MBs of 16x16 pixels so that the MBs are inputted to a plus input terminal of the subtracter 13, the motion compensation inter-frame predicting circuit 2 and the quantization step size determining circuit 12.

The motion compensation inter-frame predicting circuit 2 compares a current frame with a frame previously encoded and decoded, and while a moving amount of the MB (a moving vector) is detected, the MBs of P picture or B picture, in which inter-frame encoding is advantageous, are predicted from another frame as mentioned above. However, the MB of I picture and a MB in which intra-frame encoding is advantageous are not predicted.

In the case where an output of the block dividing circuit 1 is the MB of the I picture or the MB in which intra-frame encoding is advantageous, the switch 15 is entered to an input terminal 15b side, and the MB of the I picture is inputted from the subtracter 13 directly to the orthogonal transforming circuit 3.

Meanwhile, in the case where the output of the block dividing circuit 1 is the MB of P picture or B picture, the switch 15 is entered to an input terminal 15a side, a MB from the block dividing circuit 1 and an predicted MB from the motion compensation inter-frame predicting circuit 2 are respectively inputted to a plus and a minus input terminals of the subtracter 13, and a prediction difference (prediction error) is outputted from the subtracter 13 to the orthogonal transforming

circuit 3.

Data from the subtracter 13 (MB or prediction difference) are converted into data suitable for encoding by means of two-dimensional orthogonal transformation (discrete Fourier transformation, Hadamard transformation, discrete cosine transformation, etc.) in the orthogonal transforming circuit 3, and the transformed data are outputted to the quantizing circuit 4.

In the quantizing circuit 4, a result of the two-dimensional orthogonal transformation (namely, a transform coefficient) is quantized by using a quantization step size obtained in the quantization step size determining circuit 12, and the quantized result is outputted to the variable-length encoding circuit 5 and the inverse quantizing circuit 7.

In the variable-length encoding circuit 5, variable-length encoding is performed on the quantized transform coefficient, and the encoded transform coefficient is outputted to the buffer 6 and the bit allocating circuit 10.

The encoded data from the variable-length encoding circuit 5 are temporarily stored in the buffer 6, and the encoded data are outputted at a predetermined constant data rate therefrom.

The quantized transform coefficient is inversely quantized in the inverse quantizing circuit 7 and is outputted to the inverse orthogonal transforming circuit 8.

Reverse orthogonal transformation is carried out on the inversely quantized transform coefficient by the inverse orthogonal transforming circuit 8 so that a reconstructed value before the orthogonal transformation (MB or prediction difference) is obtained.

In the case where the reconstructed value is a prediction difference, the switch 16 is changed to an input terminal 16a side, and the prediction difference as a reconstructed value and the prediction MB outputted from the motion compensation inter-frame predicting circuit 2 are added in the adder 14 so that an MB is reconstructed. Meanwhile, in the case where the reconstructed value is an MB on which intra-frame encoding is performed, the switch 16 is changed to an input terminal 16b side so that the reconstructed value is directly outputted to the frame memory 9.

A reconstructed image obtained from the MB reconstructed in the above manner is stored in the frame memory 9. The reconstructed image is used as a reference image for inter-frame prediction in the motion compensation inter-frame predicting circuit 2.

The bit allocating circuit 10, the reference quantization step size determining circuit 11 and the quantization step size determining circuit 12 control a generating an amount of encoded data, and they have same functions and arrangements as those of a bit allocating circuit 64, a reference quantization step size determining circuit 65, and a quantization step size determining circuit 66 in a conventional image encod-

ing apparatus shown in Fig. 16.

In other words, the bit allocating circuit 10 determines a number of bits which are allocated to a frame to be encoded based upon encoded results up to the previous frame (a number of generated bits obtained from the variable-length encoding circuit 5, an average value of a quantization step size obtained from the quantization step size determining circuit 12) and a given data rate. To be concrete, as shown in the prior art, respective global complexity measures X_I , X_P and X_B of an I picture, a P picture and a B picture are determined according to the aforementioned formulas (1) through (3), and allocations of target bits T_I , T_P and T_B to images to be encoded are determined by calculating the aforementioned formulas (4) through (6) for I picture, P picture and B picture. Here, at the beginning of encoding, fixed initial values are set for the respective global complexity measures X_I , X_P and X_B .

The reference quantization step size determining circuit 11 determines a reference quantization step size of a orthogonal transformation coefficient per MB based upon a number of generated bits up to the previous MB obtained from the variable-length encoding circuit 5 and a number of bits allocated by the bit allocating circuit 10. For example, in the case of I picture, a virtual buffer fullness d_j^I in the j-th MB of the I picture is decided according to the aforementioned formula (7), and a reference quantization step size q_j^I is determined per MB according to the aforementioned formula (8). Furthermore, also in the case of P picture and B picture, reference quantization widths q_j^P and q_j^B of j-th MB are determined in the same manner as in the case of I picture. Here, at the beginning of encoding, initial buffer fullness d_0^I , d_0^P and d_0^B of respective pictures (I picture, P picture and B picture) are initialized.

The quantization step size determining circuit 12 calculates an activity for each MB which shows fineness of a picture in a MB obtained from the block dividing circuit 1, a reference quantization step size is changed by the activity per MB so as to determine a quantization step size which is used in the quantizing circuit 4 per MB. For example, in the case of I picture, a quantization step size Q_j^I of j-th MB of the I picture is determined according to the aforementioned formula (9). Moreover, also in the case of P picture and B picture, quantization widths Q_j^P and Q_j^B of j-th MB are determined in the same manner as in the case of the I picture. Here, at the beginning of encoding, an average value (avg) of the activities of the previously encoded frame is initialized.

Here, in the present embodiment, the bit allocating circuit 10, the reference quantization step size determining circuit 11 and the quantization step size determining circuit 12 constitute encoded data amount control means.

The dummy data generator 17, the switch 18 and

the controller 19 realizes prevention of underflow in the buffer 6 which is one of the objects of the present invention.

The controller 19 monitors a number of occupied bits in the buffer 6 (a number of bits of encoded data which remain in the buffer 6 in the case where the encoded data are outputted at a constant data rate after each image frame is immediately encoded and the encoded data are immediately stored in the buffer 6 in the image encoding apparatus) and switches the switch 18 to an input terminal 18a side so that the output of the buffer 6 becomes an output of the image encoding apparatus (encoded data) in the case where a number of occupied bits exceeds a fixed value Th1, and switches the switch 18 to an input terminal 18b side so that an output of the dummy data generator 17 becomes the output of the image encoding apparatus in the case where a number of occupied bits is below the fixed value Th1.

The dummy data generator 17 generates dummy data which can be discriminated on a decoder side, not shown, and be eliminated. For example, in the case where "dummy data start code" and "dummy data end code" are provided in a variable-length code list and when the switch 18 is switched to the dummy data generator 17 side, the dummy data generator 17 generates an arbitrary bit string (however, the bit string does not form "dummy data end code") successively after generating "dummy data start code", and generates "dummy data end code" just before the switch 18 is switched to the buffer 6 side. A format of the dummy data is shown in Fig. 13.

Or, a dummy code composed of a plurality of bits is set, and while the switch 18 is on the dummy data generator 17 side, the dummy data generator 17 may generate successively the above kind of the dummy codes. A format of the dummy data is shown in Fig. 14.

Or, "start code" is always inserted into the front of each frame. In the case of a encoding system which is capable of inserting bits, an arbitrary number of "0"s just after the "start code" (namely, a system where on the image encoding apparatus side, the "start code" is always inserted into the front of encoded data of each frame, and on the decoder side, bits "0" just after the "start code" (bit string) are eliminated), the controller 19 and the dummy data generator 17 may have the following functions. Namely, the controller 19 checks whether or not the "start code" is inputted from the variable-length encoding circuit 5 to the buffer 6, and monitors a number of occupied bits in the buffer 6 when the "start code" is inputted to the buffer 6. When a number of occupied bits in the buffer 6 is below a determined value Th1 and the "start code" is outputted from the buffer 6, the switch 18 is switched to the dummy data generator 17 side, and when not, switched to the buffer 6 side. The dummy data generator 17 successively generates bits "0"

(successively outputs the same bits). In this manner, a plurality of bits "0" continuously exist just after the "start code" in the encoded data, but they can be eliminated on the decoder side. A format of the dummy data is shown in Fig. 15.

The following will discuss an operation of the image encoding apparatus having the above arrangement.

First, in the block dividing circuit 1, a frame to be encoded is divided into MBs, and intra-frame encoding or inter-frame encoding is performed per MB. In the case of the intra-frame encoding, two-dimensional orthogonal transformation is carried out on the MBs from the block dividing circuit 1 by the orthogonal transforming circuit 3, whereas in the case of the inter-frame encoding, two-dimensional transformation is carried out on a difference (prediction difference) between the MBs from the block dividing circuit 1 and prediction MBs from the motion compensation inter-frame predicting circuit 2 by the orthogonal transforming circuit 3.

Next, in the quantizing circuit 4, a result of the two-dimensional orthogonal transformation by the orthogonal transform circuit 3 (transformation coefficient) is quantizing by a quantization step size obtained in the quantization step size determining circuit 12. After that, in the variable-length encoding circuit 5, variable-length encoding is performed on the quantized transform coefficient and the encoded data are temporarily stored in the buffer 6.

The controller 19 monitors a number of occupied bits in the buffer 6, and when the number of occupied bits in the buffer 6 exceeds a threshold Th1, a common output terminal of the switch 18 is connected to the input terminal 18a. In this case, the encoded data are outputted from the buffer 6 at a predetermined constant rate.

Fig. 2 shows a number of occupied bits in the buffer 6 in the case where an image 3 is encoded by the image encoding apparatus of the present embodiment (image that is shifted to a normal motion picture after frequent scene changes for continuous 30 frames). In this example, a threshold Th1 which changes the switch 18 is -10^5 bits.

In this case, the number of occupied bits in the buffer 6 is not more than the threshold Th1 at about time 27, and the switch 18 is switched to the dummy data generator 17 side by the controller 19 which monitors the number of occupied bits in the buffer 6. Therefore, from the image encoding apparatus, instead of the encoded data read out from the buffer 6, dummy data from the dummy data generator 17 are outputted. While the switch 18 is on the dummy data generator 17 side, transmission of the encoded data in the buffer 6 is temporarily suspended, so the number of occupied bits in the buffer 6 does not become smaller than the threshold Th1.

While the switch 18 is on the dummy data gener-

ator 17 side, the encoded data from the variable-length encoding circuit 5 are stored in the buffer 6. If a number of occupied bits in the buffer 6 exceeds the threshold Th1, the switch 18 is switched to the buffer 6 side by the controller 19, and the encoded data are again outputted from the buffer at a constant data rate.

Thereafter, as mentioned above, if a number of occupied bits in the buffer 6 is not more than the threshold Th1, an output of the image encoding apparatus becomes dummy data of the dummy data generator 17, and if a number of occupied bits in the buffer 6 exceeds the threshold Th1, the encoded data are outputted from the buffer 6 at a constant data rate. For this reason, a lower limit of a number of occupied bits in the buffer 6 can be limited substantially to the threshold Th1, thereby making it possible to prevent underflow of the buffer 6.

Here, allowing a number of occupied bits to be a minus value corresponds to specifying an origin of the occupied bits in the following manner. Namely, in the initial state, dummy data which can be eliminated on the decoder side are stored in the buffer 6, and a number of occupied bits at this time is defined as 0. Therefore, the threshold Th1 is allowed to be set to a smaller value than a number of occupied bits in the buffer 6 in the initial state. Generally, also in the case of a normal image, the rate control (control over an amount of generation of encoded data) is not accurate, namely, slight fluctuation occur. However, when the threshold Th1 is set to 0, even in the case where the rate control is slightly inaccurate, the switch 18 is switched to the dummy data generator 17 side and the dummy data are added to the encoded data. Reason for setting the threshold Th1 to a minus is to avoid the addition of such dummy data.

Here, only if a lot of dummy data are stored in the buffer 6 and an origin is set so that a number of occupied bits become a great minus value in the early state, the problem of underflow mentioned in problems to be solved by the invention cannot be essentially dissolved. The reason is that, for example, in a sequence where deep black images continue for a long time, the encoded data are hardly generated, so an amount of dummy data which is stored in the buffer 6 at the beginning should be greatly increased. In this case, since capacity of the buffer 6 should be enlarged greatly, there arises a problem that scale of hardware increases. Furthermore, in a sequence of an image 2 (an image which is shifted to a normal motion picture after stop motion continues for 30 frames) or the image 3, the underflow can be prevented, but a problem that quality of the image is considerably deteriorated at that time cannot be dissolved.

Therefore, an operation for obtaining minus values for a number of occupied bits in the buffer 6 absorbs slight fluctuation of the rate control in a normal sequence so that unnecessary addition of the dummy

data by the dummy data generator 17 in the present embodiment is prevented. However, needless to say, the threshold Th1 may be 0 as well as a positive value. In the case particularly where the fluctuation of the rate control in the normal sequence is small, the threshold Th1 may be 0 as well as a positive value.

Here, in the case where a normal motion picture (image 1) in which an stop motion and frequent scene change do not continue for a plurality of frames is encoded by the image encoding apparatus of the present embodiment, a number of occupied bits in the buffer 6 seldom becomes not more than the threshold Th1, so similarly to the conventional image encoding apparatus, a change in a number of occupied bits in the buffer 6 with time is shown in Fig. 17.

As mentioned above, the image encoding apparatus of the present embodiment is arranged so as to have:

the quantizing circuit 4 as quantizing means for quantizing orthogonal transform coefficient as information corresponding to image information;

the variable-length encoding circuit 5 as the variable-length encoding means for performing variable-length encoding on the quantized result;

the buffer 6 as temporary storage means for temporarily storing encoded data from the variable-length encoding circuit 5 so as to transmit the encoded data, which have been stored, outside at a fixed data rate;

the encoded data amount control means (bit allocating circuit 10, reference quantization step size determining circuit 11 and quantization step size determining circuit 12) for calculating a quantization step size of information to be encoded based upon the encoded result of the variable-length encoding circuit 5 adjusting the quantization step size for quantization in the quantizing circuit 4 according to the calculated result so as to control an amount of the encoded data;

the dummy data generator 17 as dummy data generating means for generating dummy data which can be eliminated on the decoding circuit which decodes the encoded data;

the switch 18 as switching means for switching an output of the image encoding apparatus to either the encoded data from the buffer 6 or the dummy data from the dummy data generator 17; and

the controller 19 as control means for monitoring a number of occupied bits in the buffer 6 so as to control the switch operation of the switch 18 such that the output of the image encoding apparatus becomes the encoded data from the buffer 6 when a number of occupied bits exceeds the predetermined threshold Th1 and that the output of the image encoded apparatus becomes the dummy data from the dummy data generator 17 when a number of occupied bits is not more than the threshold Th1.

With the above arrangement, when a number of

occupied bits in the buffer 6 becomes smaller than the threshold Th_1 , the dummy data from the dummy data generator 17 are outputted from the image encoded apparatus instead of the encoded data read out from the buffer 6. Since while the dummy data are being outputted, transmission of the encoded data in the buffer 6 is temporarily suspended, a lower limit of a number of occupied bits in the buffer 6 can be limited to the threshold Th_1 , thereby making it possible to prevent the underflow of the buffer 6.

[EMBODIMENT 2]

Next, the following will discuss another embodiment of the present invention in detail mainly referring to Figs. 4 and 5.

Here, for convenience of explanation, those members of the present embodiment that have the same arrangement and function, and that are mentioned in the above example are indicated by the same reference numerals and the description thereof is omitted.

Similarly to the aforementioned embodiment 1, the present embodiment controls underflow of a buffer. According to the embodiment 1, underflow of a buffer in an image encoding apparatus can be prevented, but since the encoded data stored in the buffer are increased by inserting dummy data despite of actually little generation of the encoded data, various parameters which are used for the rate control (controlling an amount of generation of the encoded data) lose their balance. For example, since global complexity measures X_I , X_P and X_B in I picture, P picture and B picture are calculated from a number of generated bits and an average quantization step size of I picture, P picture and B picture, if the dummy data are inserted into the encoded data, the global complexity measures become meaningless values. For this reason, in an example shown in Fig. 2, just after the frequent scene change is shifted to a normal motion picture (just after time 30), rate control is unstable, so it takes too time to return to the normal state which is shown in Fig. 17. Actually, turbulence in quality of an image can be seen. The present embodiment solves these problems.

Fig. 4 shows an arrangement of the main portion of the image encoding apparatus according to the present embodiment. A block dividing circuit 1, a motion compensation inter-frame predicting circuit 2, an orthogonal transforming circuit 3, a quantizing circuit 4, a variable-length encoding circuit 5, a buffer 6, an inverse quantizing circuit 7, an inverse orthogonal transforming circuit 8, a frame memory 9, a subtracter 13, an adder 14, a switch 15 and a switch 16 in the image encoding apparatus of the present embodiment that have the same arrangement and functions, and that are mentioned in the above embodiment 1 are indicated by the same reference numerals and the

description thereof is omitted.

A bit allocating circuit 210, a reference quantization step size determining circuit 211, a quantization step size determining circuit 212, a dummy data generator 217 as dummy data generating means, a switch 218 as switching means and a controller 219 as control means in the image encoding apparatus of the present embodiment adopt the method of the present invention so as to prevent underflow in the buffer 6 of the image encoding apparatus, and have a function for keeping good quality of an image.

The bit allocating circuit 210, the reference quantization step size determining circuit 211, the quantization step size determining circuit 212, the dummy data generator 217, the switch 218 and the controller 219 basically have same functions as those of the the bit allocating circuit 10, the reference quantization step size determining circuit 11, the quantization step size determining circuit 12, the dummy data generator 17 and the switch 18 and the controller 19 of the aforementioned embodiment 1 which are shown in Fig. 1, but in the present embodiment, the following operations are further added.

In other words, the controller 219 switches the switch 218 to the dummy data generator 217 side and simultaneously transmits a switch signal a which shows this operation to the bit allocating circuit 210, the reference quantization step size determining circuit 211 and the quantization step size determining circuit 212.

In the bit allocating circuit 210, the reference quantization step size determining circuit 211 and the quantization step size determining circuit 212, when the switch signal a is inputted from the controller 219, a parameter which is used for the rate control is initialized. In other words, when the switch signal a is inputted to the bit allocating circuit 210, the global complexity measures X_I , X_P and X_B of each picture (I picture, P picture and B picture) are initialized (set to an initial value). Moreover, when the switch signal a is inputted to the reference quantization step size determining circuit 211, initial buffer fullness d_0^I , d_0^P , d_0^B of each picture (I picture, P picture and B picture) are initialized (set to an initial value). Furthermore, when the switch signal a is inputted to the quantization step size determining circuit 212, an average value avg of the activities in the previous frame is initialized (set to an initial value).

Here, in the present embodiment, the bit allocating circuit 210, the reference quantization step size determining circuit 211 and the quantization step size determining circuit 212 constitute the encoded data amount control means.

With the above arrangement, the following will discuss an operation of the image encoding apparatus of the present embodiment.

As mentioned in the aforementioned embodiment 1, the controller 219 monitors a number of oc-

cupied bits in the buffer 6 and judges whether or not the number of occupied bits in the buffer 6 exceeds the threshold Th1. When the number of occupied bits in the buffer 6 exceeds the threshold Th1, the controller 219 switches the switch 218 to the buffer 6 side and encoded data are outputted from the buffer 6 at a predetermined constant data rate.

Fig. 5 shows a number of occupied bits in the buffer 6 in the case where an image 3 (an image which is shifted to a normal motion picture after frequent scene change continues for 30 frames) is encoded by the image encoding apparatus of the present embodiment. Also in this case, the threshold Th1 which switches the switch 218 is 10^5 bits.

In this case, the number of occupied bits in the buffer 6 becomes not more than the threshold Th1 at about time 27. Then, the switch 218 is switched to the dummy data generator 217 side by the controller 219 which monitors the number of occupied bits in the buffer 6 and at the same time, the switch signal *a* is outputted from the controller 219 to the bit allocating circuit 210, the reference quantization step size determining circuit 211 and the quantization step size determining circuit 212.

Therefore, dummy data from the dummy data generator 217 are outputted from the image encoding apparatus instead of the encoded data read out from the buffer 6, and while the dummy data is being outputted, transmission of the encoded data in the buffer 6 is suspended, so the number of occupied bits in the buffer 6 does not become less than the threshold Th1. Moreover, when an output of the dummy data is started, a parameter which is used for the rate control is initialized in the bit allocating circuit 210, the reference quantization step size determining circuit 211 and the quantization step size determining circuit 212. For this reason, even when the dummy data are inserted into the encoded data, the parameter for the rate control, which is used for calculating a quantization step size, can keep its balance.

While the switch 218 is on the dummy data generator 217 side, the encoded data from the variable-length encoding circuit 5 are stored in the buffer 6. If the number of occupied bits in the buffer 6 exceeds the threshold Th1, the switch 218 is switched to the buffer 6 side by the controller 219 and the encoded data are again outputted from the buffer 6 at a constant data rate.

Subsequently, in the same manner as in the above, if the number of occupied bits in the buffer 6 becomes not more than the threshold Th1, transmission of the encoded data stored in the buffer 6 is suspended so that the dummy data are outputted instead of the encoded data and a parameter which is used for the rate control is initialized. Thereafter, if the number of occupied bits in the buffer 6 exceeds the threshold Th1, the encoded data are outputted from the buffer 6 at a constant rate. For this reason, a lower

limit of the number of occupied bits in the buffer 6 can be substantially limited to the threshold Th1. As a result, the underflow of the buffer 6 can be prevented and also the parameter for the rate control during the insertion of the dummy data can keep its balance.

It is apparent from Fig. 5 that the underflow of the buffer 6 can be prevented, and the normal rate control is worked just after the image is shifted to the normal motion picture. In other words, in the aforementioned embodiment 1, as shown in Fig. 2, the number of occupied bits in the buffer 6 becomes repeatedly not more than the threshold Th1 even after time 30, and the dummy data are inserted by the present invention. However, in the present embodiment, as shown in Fig. 5, a configuration of the graph just after time 30 is same as that of the normal motion picture (Fig. 17), namely, it is returned to a normal state.

Similarly to the image encoding apparatus of the embodiment 1, the image encoding apparatus of the present embodiment is arranged so as to have:

the dummy data generator 217 as dummy data generating means for generating dummy data which can be eliminated on the decoding circuit which decodes encoded data;

the switch 218 as switching means for switching an output of the image encoding apparatus to either the encoded data from the buffer 6 or the dummy data from the dummy data generator 217; and

the controller 219 as control means for monitoring a number of occupied bits in the buffer 6 and controlling the switching operation of the switch 218 so that the output of the image encoding apparatus becomes the encoded data from the buffer 6 when a number of occupied bits exceeds the predetermined threshold Th1 and that the output of the image encoded apparatus becomes the dummy data from the dummy data generator 217 when a number of occupied bits is not more than the threshold Th1. Furthermore, the image encoding apparatus of the present embodiment is arranged so that when the number of occupied bits in the buffer 6 is not more than the threshold Th1, the switch signal *a* is outputted to the bit allocating circuit 210, the reference quantization step size determining circuit 211 and the quantization step size determining circuit 212 as the encoded data amount control means by the controller 219, and when the switch signal *a* is inputted, the bit allocating circuit 210, the reference quantization step size determining circuit 211 and the quantization step size determining circuit 212 initialize various parameters for the rate control (various parameters which are used for calculating a quantization step size).

With the above arrangement, the underflow of the buffer 6 can be prevented in the same way as in the embodiment 1, and even when the dummy data are outputted instead of the actual encoded data, various parameters which are used for the rate control keep their balance and the constant rate control can

be realized, thereby making it possible to code image information with good quality.

[EMBODIMENT 3]

Next, the following will discuss a third embodiment of the present invention mainly referring to Figs. 6 and 7.

Here, for convenience of explanation, those members of the present embodiment that have the same arrangement and function, and that are mentioned in the above embodiments are indicated by the same reference numerals and the description thereof is omitted.

The image encoding apparatus of the present embodiment controls overflow of a buffer which is one of the problems in the prior arts, and an arrangement of its main circuit is shown in Fig. 6.

The block dividing circuit 1, the motion compensation inter-frame predicting circuit 2, the orthogonal transforming circuit 3, the quantizing circuit 4, the variable-length encoding circuit 5, the buffer 6, the inverse quantizing circuit 7, the inverse orthogonal transforming circuit 8, the frame memory 9, the bit allocating circuit 10, the reference quantization step size determining circuit 11, the quantization step size determining circuit 12, the subtracter 13, the adder 14, the switch 15 and the switch 16 in the image encoding apparatus of the present embodiment that have the same arrangement and functions, and that are mentioned in the above embodiment 1 are indicated by the same reference numerals and the description thereof is omitted.

The image encoding apparatus of the present embodiment includes a bit allocation changing circuit 301 as bit allocation changing means in order to prevent overflow of a buffer. When bit allocation T_I (in the case of I picture), T_P (in the case of P picture) or T_B (in the case of B picture) is inputted from a bit allocating circuit 10, the bit allocation changing circuit 301 inspects a number of occupied bits in a buffer 6 and changes the bit allocation so that a sum of the number of occupied bits in the buffer 6 and the bit allocation T_I , T_P or T_B for a frame to be encoded does not exceed a predetermined fixed value.

In other words, when the bit allocation T_I (in the case of I picture), T_P (in the case of P picture) or T_B (in the case of B picture) for a frame is inputted from the bit allocating circuit 10, a check is made as to whether or not conditions of the following formulas (11) through (13) are satisfied in the bit allocation changing circuit 301.

$$BO + T_I > ThI \dots (11) \text{ (in the case of I picture)}$$

$$BO + T_P > ThP \dots (12) \text{ (in the case of P picture)}$$

$$BO + T_B > ThB \dots (13) \text{ (in the case of B picture)}$$

Here, in the formulas (11) through (13), BO is a number of occupied bits in the buffer 6, and ThI, ThP

or ThB is a threshold which is determined for each picture.

When the conditions of the formulas (11) through (13) are not satisfied, the bit allocation changing circuit 301 outputs a value of the bit allocation, whereas when the conditions of the formulas (11) through (13) are satisfied, the bit allocation changing circuit 301 changes the values of the bit allocation T_I (in the case of I picture), T_P (in the case of P picture) or T_B (in the case of B picture) are changed according to the following formulas (14) through (16).

$$T_I = ThI - BO \dots (14) \text{ (in the case of I picture)}$$

$$T_P = ThP - BO \dots (15) \text{ (in the case of P picture)}$$

$$T_B = ThB - BO \dots (16) \text{ (in the case of B picture)}$$

With the above arrangement, the following will discuss an operation of the image encoding apparatus of the present embodiment.

Every time when encoding of one frame is completed, in the bit allocating circuit 10, a number of bits which are allocated to a frame to be encoded, namely, the bit allocation T_I (in the case of I picture), T_P (in the case of P picture) or T_B (in the case of B picture) is calculated according to encoded results up to the previous frame (a number of generated bits obtained from the variable-length encoding circuit 5 and an average value of a quantization step size obtained from the quantization step size determining circuit 12), and the calculated value is outputted to the bit allocation changing circuit 301.

When the bit allocation is inputted, a check is made whether or not the conditions of the formulas (11) through (13) are satisfied in the bit allocation changing circuit 301. If the conditions are not satisfied, the value of the bit allocation is directly outputted to the reference quantization step size determining circuit 11, and if the conditions are satisfied, the value of the bit allocation is changed according to the formulas (14) through (16) and the changed bit allocation is outputted to the reference quantization step size determining circuit 11.

Fig. 7 shows a number of occupied bits in the buffer 6 in the case where an image 2 (an image which is shifted to a normal motion picture after stop motion continues for 30 frames) is encoded by the image encoding apparatus of the present embodiment. In this example, all thresholds ThI, ThP and ThB are set to 8×10^5 .

In this case, since new GOP starts in a stop motion at time 15 and an I picture appears, the bit allocation T_I which is calculated in the bit allocating circuit 10 becomes great unusually and $BO + T_I$ exceeds the threshold ThI. As a result, the condition of the formula (11) is satisfied. For this reason, the bit allocation changing circuit 301 changes the bit allocation according to the formula (14) so that $BO + T_I$ does not exceed the threshold ThI. Therefore, even if the I picture which appears at time 15 is encoded and stored to the buffer 6, the number of occupied bits in the buf-

fer 6 does not considerably exceed the threshold ThI, so the overflow is prevented.

In addition, since generation of a lot of encoded data in an I picture which appears at time 15 are restrained, a number of remained bits in GOP can be secured, and an usual number of bits is allocated to the frames thereafter in the GOP. Therefore, it is also possible to restrain deterioration of quality of an image.

Effects of prevention of the overflow are quite obvious by comparing the graphs (solid line) for the image 2 in Figs. 7 and 18.

As mentioned above, the image encoding apparatus of the present invention is arranged so as to have the bit allocation changing circuit 301 as the bit allocation changing means for monitoring a number of occupied bits in the buffer 6 so as to change the calculated bit allocation when the sum of bit allocation to a frame which has been calculated before encoding and a number of occupied bits in the buffer 6 at the time of the calculation of bit allocation exceeds the predetermined threshold ThI, ThP or ThB, such that the sum does not exceed the threshold.

For this reason, even if information of the frame is encoded and stored to the buffer 6, a number of occupied bits in the buffer 6 at that time does not considerably exceed the thresholds, so if the thresholds are set to smaller values than a storage capacity of the buffer 6, the overflow can be prevented.

[EMBODIMENT 4]

The following will discuss a fourth embodiment of the present invention mainly referring to Figs. 8 through 10.

Here, for convenience of explanation, those members of the present embodiment that have the same arrangement and function, and that are mentioned in the above embodiments are indicated by the same reference numerals and the description thereof is omitted.

Similarly to the embodiment 3, the image encoding apparatus of the present embodiment also controls overflow of a buffer, but further improves the effects of the prevention of overflow in embodiment 3.

An arrangement of a main circuit in the image encoding apparatus of the present embodiment is shown in Fig. 8. A block dividing circuit 1, a motion compensation inter-frame predicting circuit 2, an orthogonal transforming circuit 3, a quantizing circuit 4, a variable-length encoding circuit 5, a buffer 6, an inverse quantizing circuit 7, an inverse orthogonal transforming circuit 8, a frame memory 9, a bit allocating circuit 10, a reference quantization step size determining circuit 11, a quantization step size determining circuit 12, a subtracter 13, an adder 14, a switch 15, a switch 16 and a bit allocation changing circuit 301 in the image encoding apparatus of the

present embodiment that have the same arrangement and functions, and that are mentioned in the above embodiment 3 are indicated by the same reference numerals and the description thereof is omitted.

The image encoding apparatus of the present embodiment have a quantization step size changing circuit 401 as quantization step size changing means in order to effectively prevent overflow of the buffer 6. When data of a quantization step size are inputted from the quantization step size determining circuit 12, the quantization step size changing circuit 401 inspects a number of occupied bits in the buffer 6, and if the number of occupied bits in the buffer 6 exceed predetermined threshold, the quantization step size changing circuit 401 changes the quantization step size which has been determined in the quantization step size determining circuit 12 to a greater value.

In other words, the quantization step size changing circuit 401 changes the quantization step size by multiplying a value α shown in the following formula (17) or (18) by quantization widths Q_j^I , Q_j^P and Q_j^B in j-th MB of each picture which have been determined in the quantization step size determining circuit 12.

$$\alpha = 1 + k(BO - C) \text{ (when } BO > C) \quad (17)$$

$$\alpha = 1 \text{ (when } BO \leq C) \quad (18)$$

In the formula (17), k and C are constants ($k > 0$, $C > 0$). A relationship between α and a number of occupied bits BO is shown in Fig. 9. As shown in the example, α may linearly increase when BO is bigger than C but it is not limited to this. For example, α may be represented by a curve such that α gradually becomes bigger than 1 with increase in BO when BO is smaller than C, and rapidly becomes bigger than 1 when BO exceeds C.

In the above arrangement, the following will discuss an operation of the image encoding apparatus of the present embodiment.

In the same manner as in embodiment 3, the bit allocation T_I , T_P or T_B calculated in the bit allocating circuit 10 is inputted, the bit allocating changing circuit 301 changes a value of the bit allocation so that the sum of a number of occupied bits in the buffer 6 and the bit allocation T_I , T_P or T_B does not exceed a predetermined constant value.

Thereafter, in the reference quantization step size determining circuit 11 and the quantization step size determining circuit 12, quantization widths are calculated per MB based upon the value of the bit allocation from the bit allocation changing circuit 301 and activity per MB, and the calculated results are outputted to the quantization step size changing circuit 401.

In the quantization step size changing circuit 401, a number of occupied bits in the buffer 6 BO is checked every time when the data of a quantization step size are inputted from the quantization step size determining circuit 12, and when the number of occu-

pied bits in the buffer 6 BO exceeds the threshold C, the quantization widths are increased by multiplying α obtained by the calculation of the formula (17) by the quantization widths.

Fig. 10 shows a number of occupied bits in the buffer 6 in the case where an image 2 (an image which is shifted to a normal motion picture after the stop motion continues for 30 frames) is encoded by the image encoding apparatus of the present embodiment. In this example, $k = 3.1 \times 10^{-4}$, $C = 8 \times 10^5$, and ThI, ThP and ThB are all 8×10^5 . From Fig. 10, it is obvious that overflow of the buffer 6 is prevented more efficiently than in embodiment 3.

As mentioned above, the image encoding apparatus of the present embodiment having the arrangement of embodiment 3 is arranged so as to further include the quantization step size changing circuit 401 as the quantization step size changing means for monitoring a number of occupied bits in the buffer 6 BO so as to change the quantization widths calculated in the quantization step size determining circuit 12 to a greater value by multiplying α by the quantization widths when the number of occupied bits BO exceeds the predetermined threshold C.

Therefore, not only the bit allocation is changed as mentioned in embodiment 3, when the number of occupied bits in the buffer 6 BO exceeds the threshold C, but also the quantization step size is changed to a greater value, thereby making it possible to prevent the overflow in the buffer 6 more efficiently than in embodiment 3.

Here, in the present embodiment, the quantization step size is increased by multiplying α by the quantization step size, but the present embodiment is not limited to this, so the quantization step size may be increased by adding a certain value or changing a function $f(Q)$ (Q is a quantization step size) where the relationship: $f(Q) > Q$ holds. Needless to say, the processes for increasing the quantization step size are performed in the case of $BO > C$.

In embodiments 1 through 4, a encoding method using arts, such as orthogonal transformation, motion compensation inter-frame prediction, is adopted, but the present invention can be applied to a encoding method using arts other than the above.

In addition, all or parts of the methods described in embodiments 1 through 4 are used simultaneously so that underflow or overflow of a buffer can be prevented. For example, Fig. 11 is a block diagram which shows an example of a encoding method including all the methods mentioned in embodiments 1 through 4. The image encoding apparatus in Fig. 11 that have the same arrangement and function, and that are mentioned in the above embodiments 1 through 4 are indicated by the same reference numerals and the description thereof is omitted.

A solid line and a broken line in Fig. 12 respectively show a number of occupied bits in the buffer 6 in

the case where the image 2 and the image 3 are encoded by the image encoding apparatus in Fig. 11. Here, the threshold ThI which makes the controller 219 change the switch 218 is 10^5 bits, all the thresholds ThI, ThP and ThB of each picture which becomes a reference when the bit allocation per frame is changed are 8×10^5 , and the constant k in the formula (17) is 3.1×10^{-4} and C is 8×10^5 . From Fig. 12, it is obvious that the underflow and overflow of the buffer 6 is prevented efficiently.

The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

Claims

1. An image encoding apparatus, comprising:
 - quantizing means for quantizing information which corresponds to an image;
 - variable-length encoding means for performing variable-length encoding on the quantized result of said quantizing means;
 - temporary storage means for temporarily storing encoded data from said variable-length encoding means so as to transmit the stored encoded data to an outside at a fixed data rate;
 - encoded data amount control means for calculating a quantization step size of quantizing information to be encoded based upon the encoded result of said variable-length encoding means so as to control an amount of the encoded data of said variable-length encoding means;
 - dummy data generating means for generating dummy data which can be eliminated on a decoding circuit for decoding the encoded data;
 - switching means for switching an output of said image encoding apparatus to either the encoded data from said temporary storage means or to the dummy data from said dummy data generating means; and
 - control means for monitoring a number of occupied bits in said temporary storage means so as to control a switching operation of said switching means so that the output of the image encoding apparatus becomes the encoded data from said temporary storage means when the number of occupied bits exceeds a predetermined threshold, whereas so as to suspend transmission of data in said temporary storage means and control the switching operation of said switching means so that the output of the image encoding apparatus becomes the dummy data generated from said dummy data generating

means when the number of occupied bits is not more than the threshold.

2. The image encoding apparatus as defined in claim 1, wherein:

said control means outputs a switching signal into said encoded data amount control means when the number of occupied bits is not more than the thresholds; and

said encoded data amount control means initializes various parameters which are used for calculation of the quantization step size when the switching signal is inputted.

3. The image encoding apparatus as defined in claim 2, wherein said encoded data amount control means includes:

bit allocating means for calculating a degree of complexity in an image of a frame to be encoded from the encoded results up to the previous frame so as to determine a number of bits to be allocated to the frame to be encoded from the degree of complexity;

reference quantization step size determining means for calculating a virtual buffer fullness based upon a number of generated bits obtained from said variable-length encoding means and a number of bits allocated by said bit allocating means so as to determine a reference quantization step size from the virtual buffer fullness; and

quantization step size determining means for calculating activities showing fineness of a picture of an image so as to determine a quantization step size which is used in the quantizing means by changing the reference quantization step size based upon activities of an image to be encoded and an average value of the activities of the frame previously encoded,

wherein the parameters which are initialized when the switching signal is inputted to said encoded data amount control means are the degree of complexity, the initial virtual buffer fullness and the average value of the activities on the previous frame.

4. The image encoding apparatus as defined in claim 1, further comprising:

block dividing means for dividing one frame of the inputted image into a plurality of macroblocks; and

two-dimensional orthogonal transforming means for carrying out two-dimensional orthogonal transformation on an output of said block dividing means,

wherein said quantizing means quantizes an output of said two-dimensional orthogonal transforming means.

5. The image encoding apparatus as defined in claim 4, further comprising:

motion compensation inter-frame predicting means for while calculating a motion vector of each macroblock by comparing a current frame with another frame, predicting a macroblock in the current frame from another frame,

wherein intra-frame encoding is performed on a frame of I picture which appears at predetermined frame intervals and inter-frame prediction encoding is performed on a frame of pictures other than the I picture.

6. The image encoding apparatus as defined in claim 5, further comprising:

subtracting means for obtaining a difference between image data which have been predicted by said motion compensation inter-frame predicting means and current input image data,

wherein in the case where inter-frame prediction encoding is performed, two-dimensional orthogonal transformation is carried out on the prediction difference obtained in said subtracting means by said two-dimensional orthogonal transforming means and the transformed prediction difference is quantized by said quantizing means.

7. The image encoding apparatus as defined in claim 5, wherein said motion compensation inter-frame predicting means includes:

inverse quantizing means for inversely quantizing the output of said quantizing means;

inverse orthogonal transforming means for carrying out inverse orthogonal transformation on the output of said inverse quantizing means;

a frame memory for storing image data which have been reconstructed by said inverse orthogonal transforming means; and

motion compensation predicting circuit for calculating a motion vector from reconstructed image data in said frame memory and current input image data so as to predict a macroblock of a current frame.

8. The image encoding apparatus as defined in claim 1, wherein said dummy data generating means generates dummy data with an arbitrary data length which include a dummy data start code showing a start of the dummy data and a dummy data end code showing an end of the dummy data.

9. The image encoding apparatus as defined in claim 1, wherein said dummy data generating means successively generates predetermined dummy codes composed of a plurality of bits.

10. The image encoding apparatus as defined in claim 1, wherein:

said variable-length encoding means adds a predetermined start code to a front of each frame,

said dummy data generating means generates dummy data where same bits continue,

said control means controls a switching operation of the switching means immediately after the start code is outputted from said temporary storage means so that the dummy data are outputted from said dummy data generating means successively after generating the start code in the case where the output of the image encoding apparatus is switched to the dummy data.

11. The image encoding apparatus as defined in claim 1, wherein:

said temporary storage means stores a predetermined amount of dummy data which can be eliminated on a decoding circuit in an initial state,

the thresholds are set to smaller values than the number of occupied bits in said temporary storage means in an initial state.

12. An image encoding apparatus, comprising:

quantizing means for quantizing information which corresponds to an image;

variable-length encoding means for performing variable-length encoding on the quantized result of said quantizing means;

temporary storage means for temporarily storing encoded data from said variable-length encoding means so as to transmit the stored encoded data to an outside at a fixed data rate; and

encoded data amount control means for calculating bit allocation per frame of information to be encoded based upon the encoded result of said variable-length encoding means, and calculating a quantization step size from the above calculated result, and adjusting the quantization step size of quantization in said quantizing means according to the above calculated result so as to control an amount of the encoded data of said variable-length encoding means,

wherein said encoded data amount control means includes bit allocation changing means for monitoring a number of occupied bits in the temporary storage means so as to change the calculated bit allocation when the sum of bit allocation to a frame which has been calculated before encoding and a number of occupied bits in said temporary storage means at the time of the calculation of the bit allocation exceeds a predetermined threshold, such that the sum does not exceed the threshold.

13. The image encoding apparatus as defined in claim 12, wherein said encoded data amount control means includes:

bit allocating means for calculating a degree of complexity in an image of a frame to be encoded from the encoded results up to the previous frame so as to determine a number of bits to be allocated to the frame to be encoded from the degree of complexity;

said bit allocation changing means for changing the bit allocation obtained by said bit allocating means;

reference quantization step size determining means for calculating a virtual buffer fullness based upon the number of generated bits obtained from said variable-length encoding means and the bit allocation changed by said bit allocation changing means so as to determine a reference quantization step size from the virtual buffer fullness; and

quantization step size determining means for calculating activities showing fineness of a picture of an image so as to determine a quantization step size which is used in the quantization step size determining circuit by changing the reference quantization step size based upon activities of an image to be encoded and an average value of the activities of the frame to be previously encoded.

14. The image encoding apparatus as defined in claim 12, wherein said bit allocation changing means changes the bit allocation to a value obtained by subtracting the number of occupied bits from the threshold when the sum of the bit allocation to the frame calculated before encoding and the number of occupied bits in the temporary storage means at the time of calculation of the bit allocation exceeds the predetermined threshold.

15. The image encoding apparatus as defined in claim 12, further comprising:

block dividing means for dividing one frame of the inputted image into a plurality of macroblocks; and

two-dimensional orthogonal transforming means for carrying out two-dimensional orthogonal transformation on an output of said block dividing means,

wherein said quantizing means quantizes an output of said two-dimensional orthogonal transforming means.

16. The image encoding apparatus as defined in claim 15, further comprising:

motion compensation inter-frame predicting means for while calculating a motion vector of each macroblock by comparing a current frame

with another frame, predicting a macroblock of the current frame from another frame,

old.

wherein intra-frame encoding is performed on a frame of an I picture which appears at predetermined frame intervals and inter-frame prediction encoding is performed on a frame of pictures other than the I picture.

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17. The image encoding apparatus as defined in claim 16, further comprising:

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subtracting means for obtaining a difference between image data which have been predicted by said motion compensation inter-frame predicting means and current input image data,

wherein in the case where inter-frame prediction encoding is performed, two-dimensional orthogonal transformation is carried out on the prediction difference obtained in said subtracting means by said two-dimensional orthogonal transforming means and the transformed prediction difference is quantized by said quantizing means.

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18. The image encoding apparatus as defined in claim 16, wherein said motion compensation inter-frame predicting means includes:

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inverse quantizing means for inversely quantizing the output of said quantizing means;

inverse orthogonal transforming means for carrying out inverse orthogonal transformation on the output of said inverse quantizing means;

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a frame memory for storing image data which have been reconstructed by said inverse orthogonal transforming means; and

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motion compensation predicting circuit for calculating a motion vector from the reconstructed image data in said frame memory and current input image data so as to predict a macroblock of a current frame.

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19. The image encoding apparatus as defined in claim 12, wherein said encoded data amount control means further includes quantization step size changing means for monitoring a number of occupied bits in said temporary storage means so as to change the calculated quantization step size to a greater value when the number of occupied bits exceeds the predetermined threshold.

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20. An image encoding apparatus in which image data is quantized and variable-length encoded and then stored into a temporary storage means for fixed data rate transmission, and in which dummy data which can be eliminated on decoding is output from the apparatus when it is detected that the occupied space in the temporary storage means is less than a predetermined thresh-

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FIG. 1

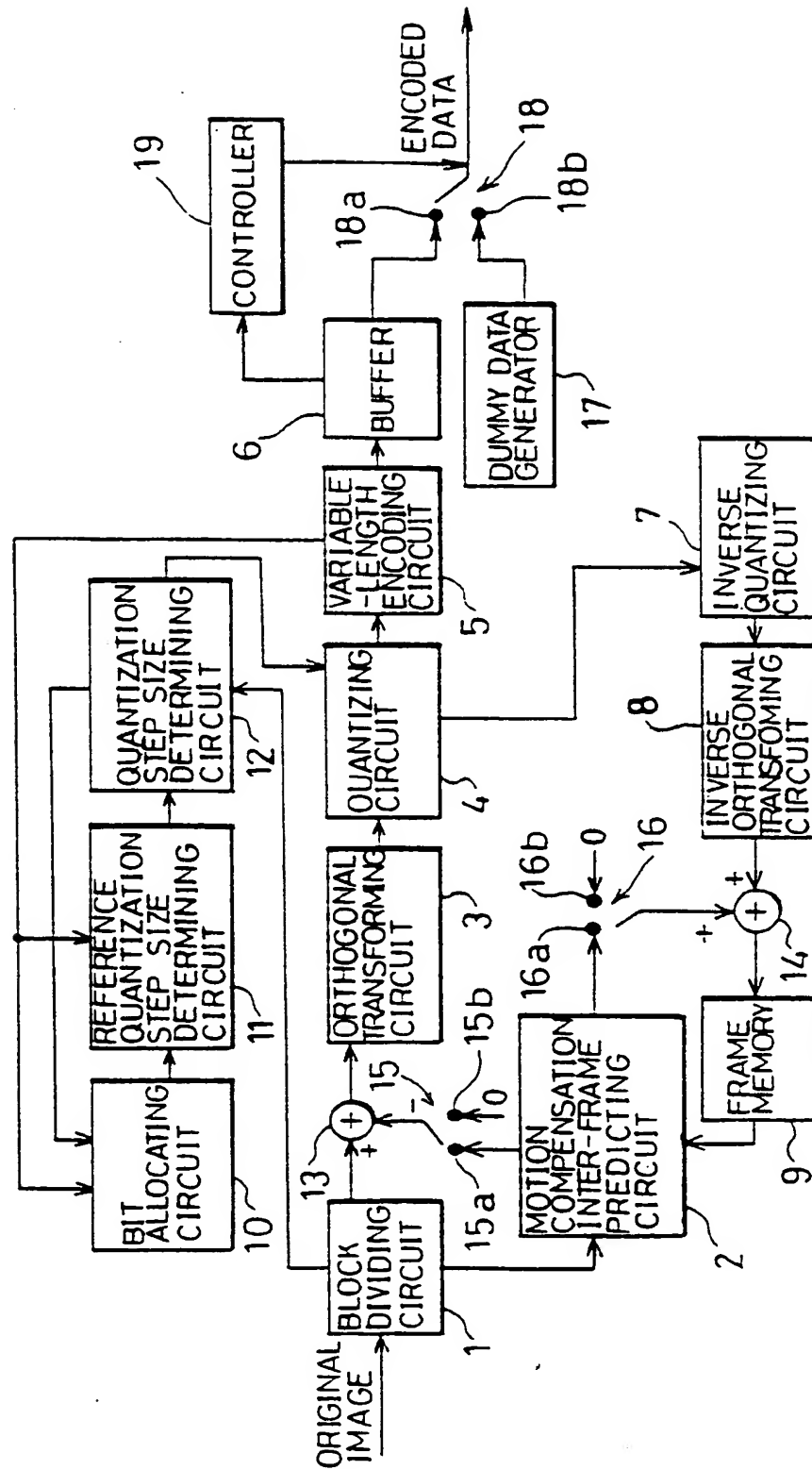


FIG. 2

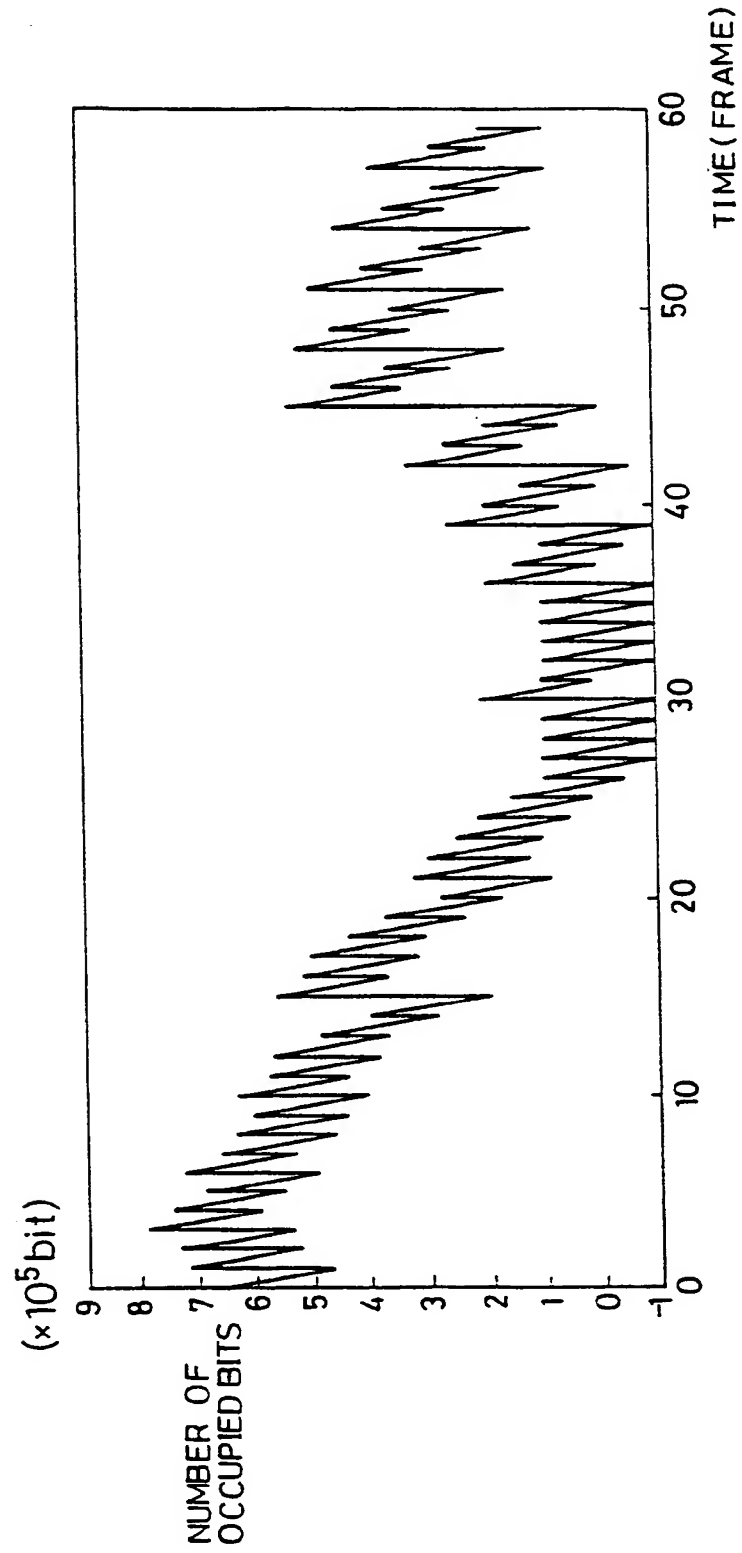


FIG. 3

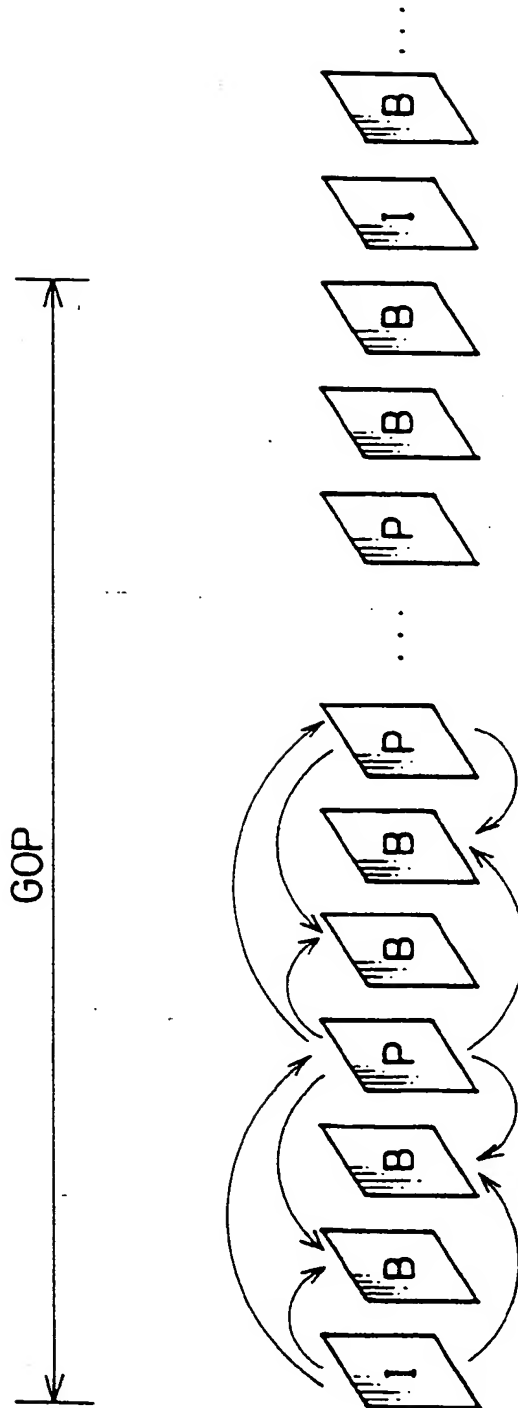


FIG. 4

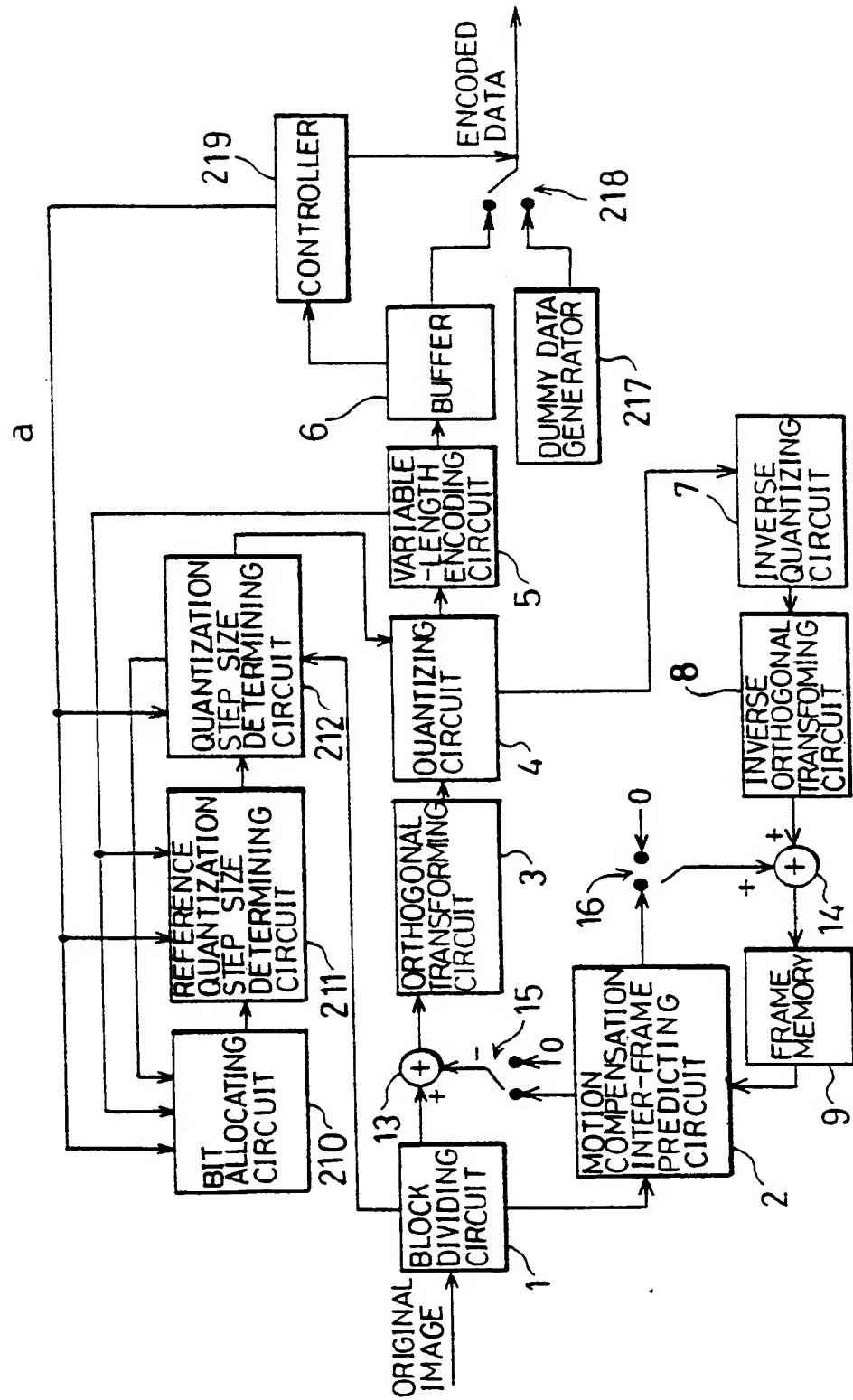


FIG. 5

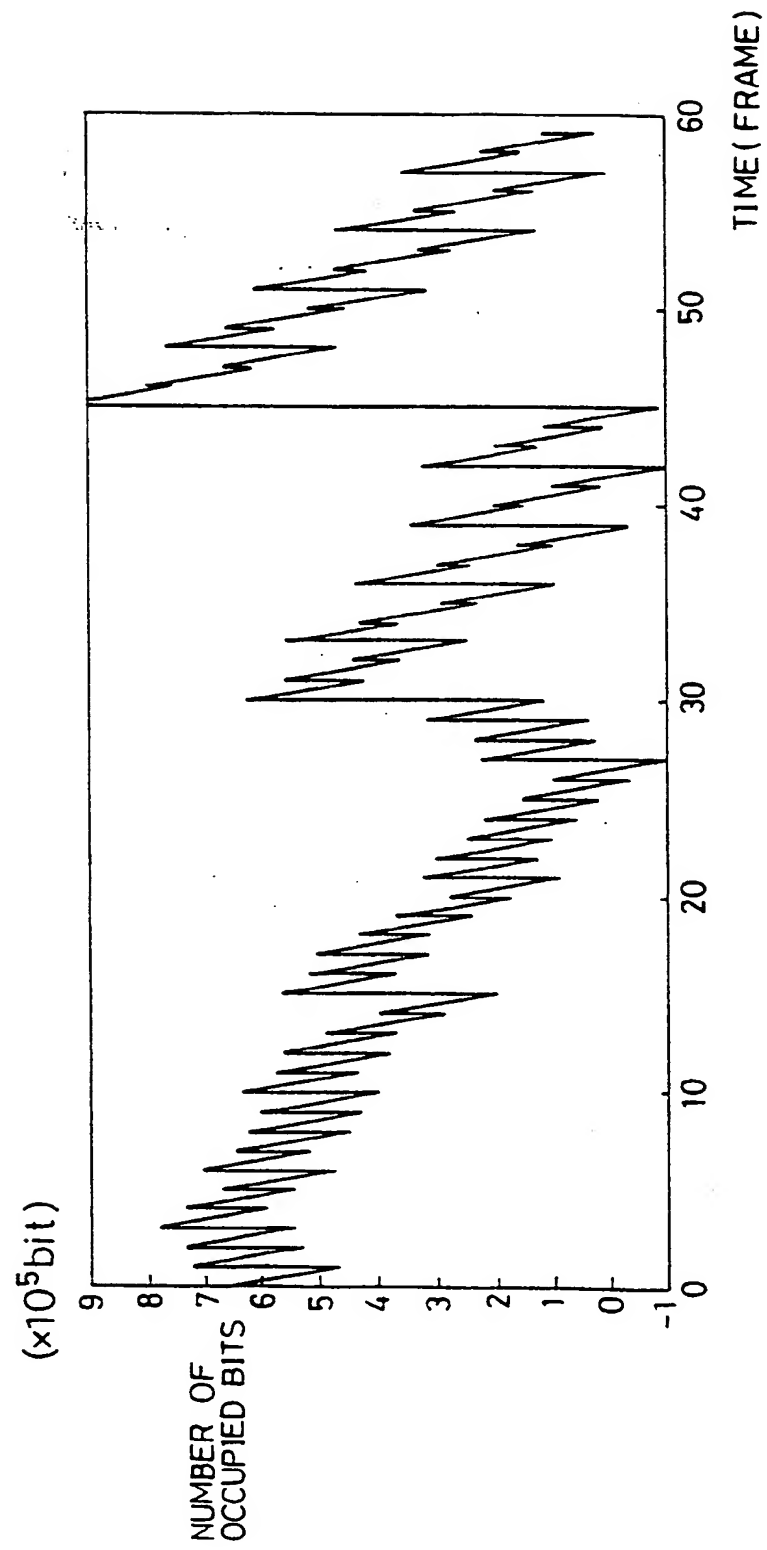
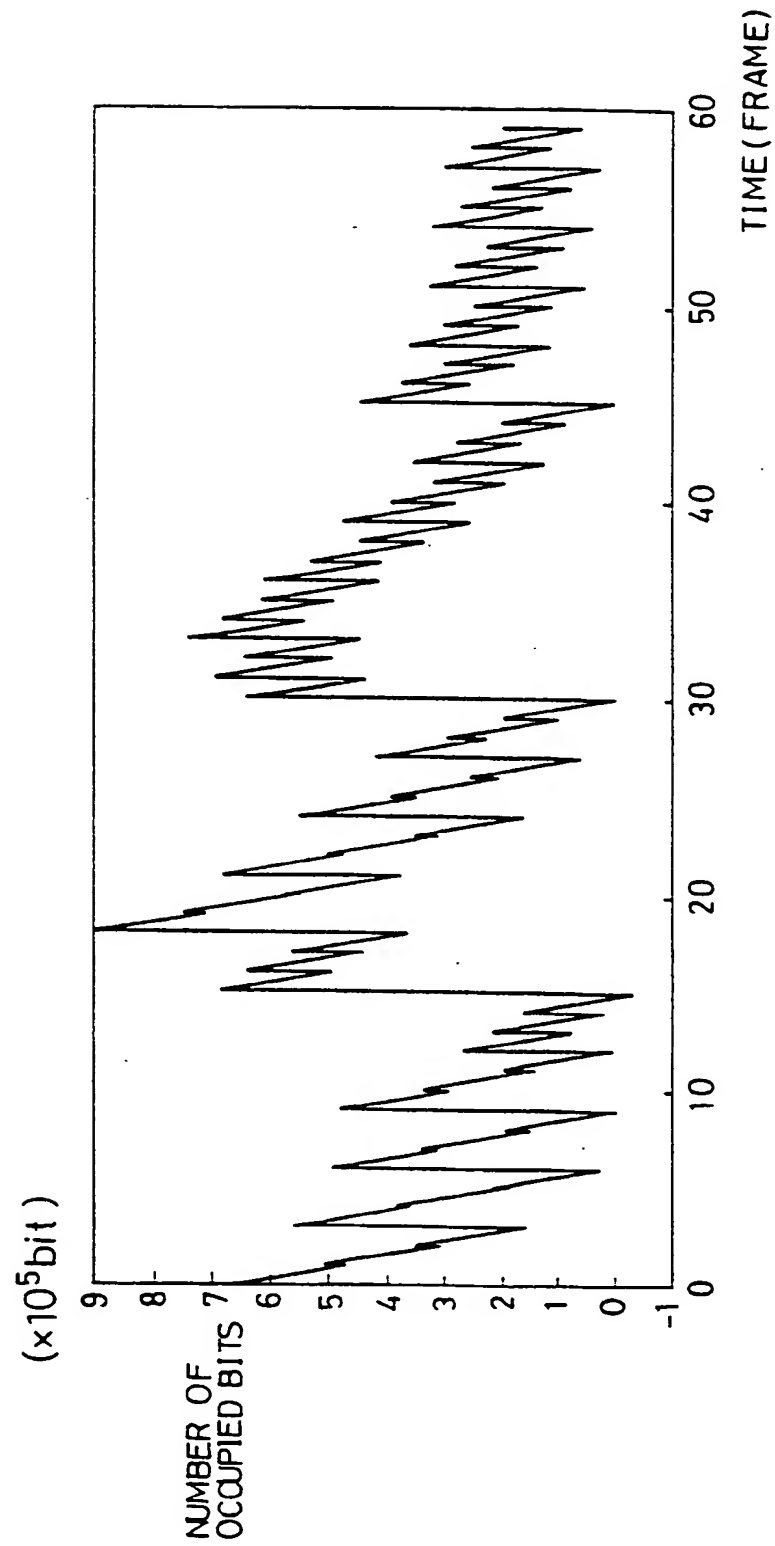


FIG. 7



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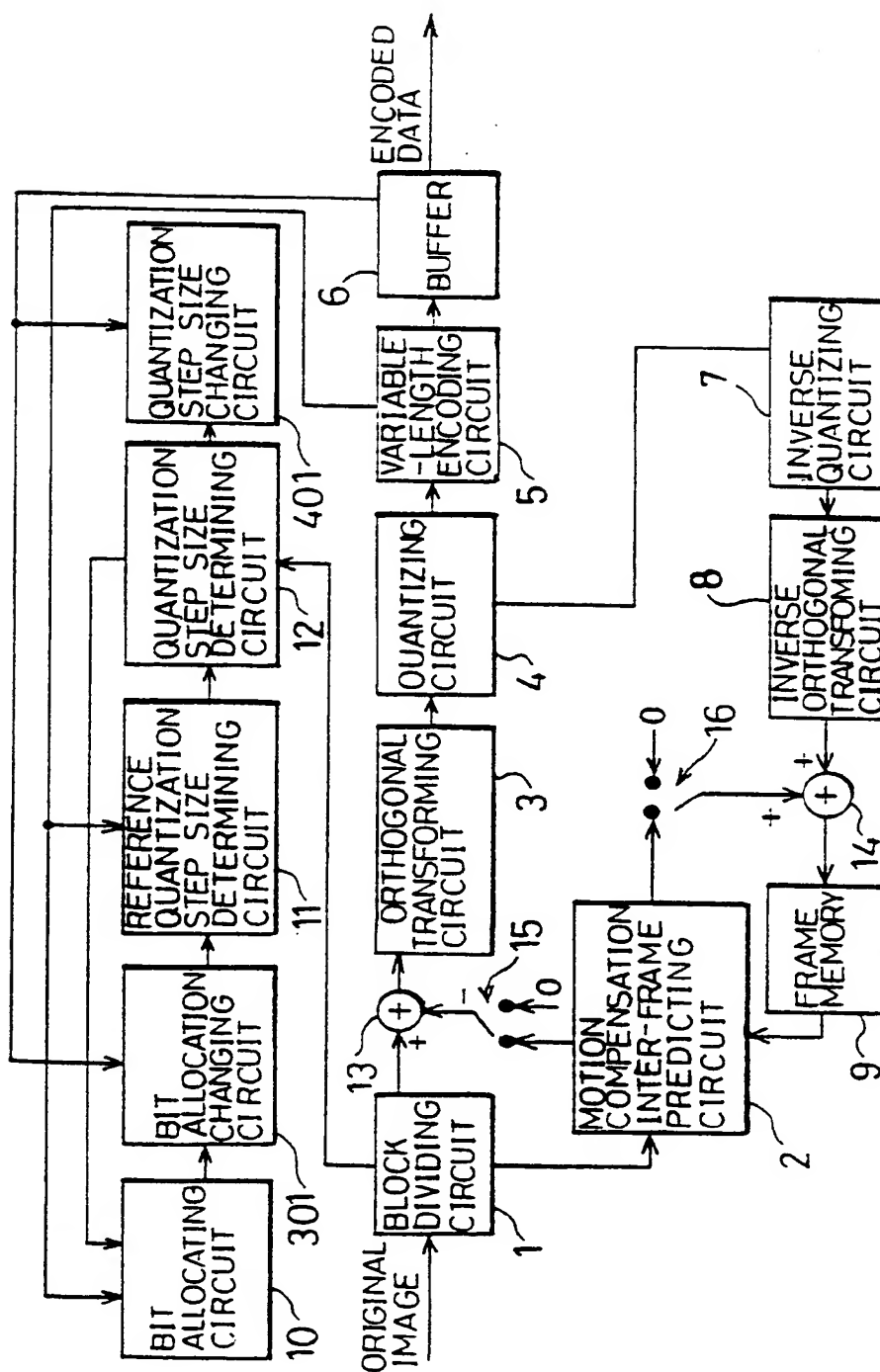


FIG. 9

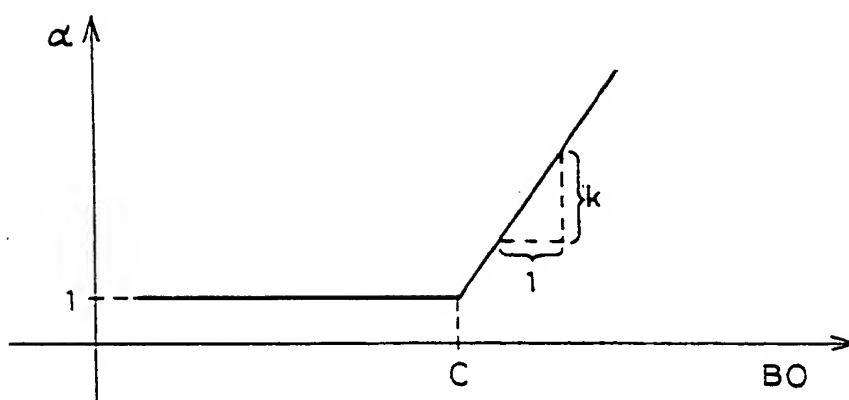


FIG. 10

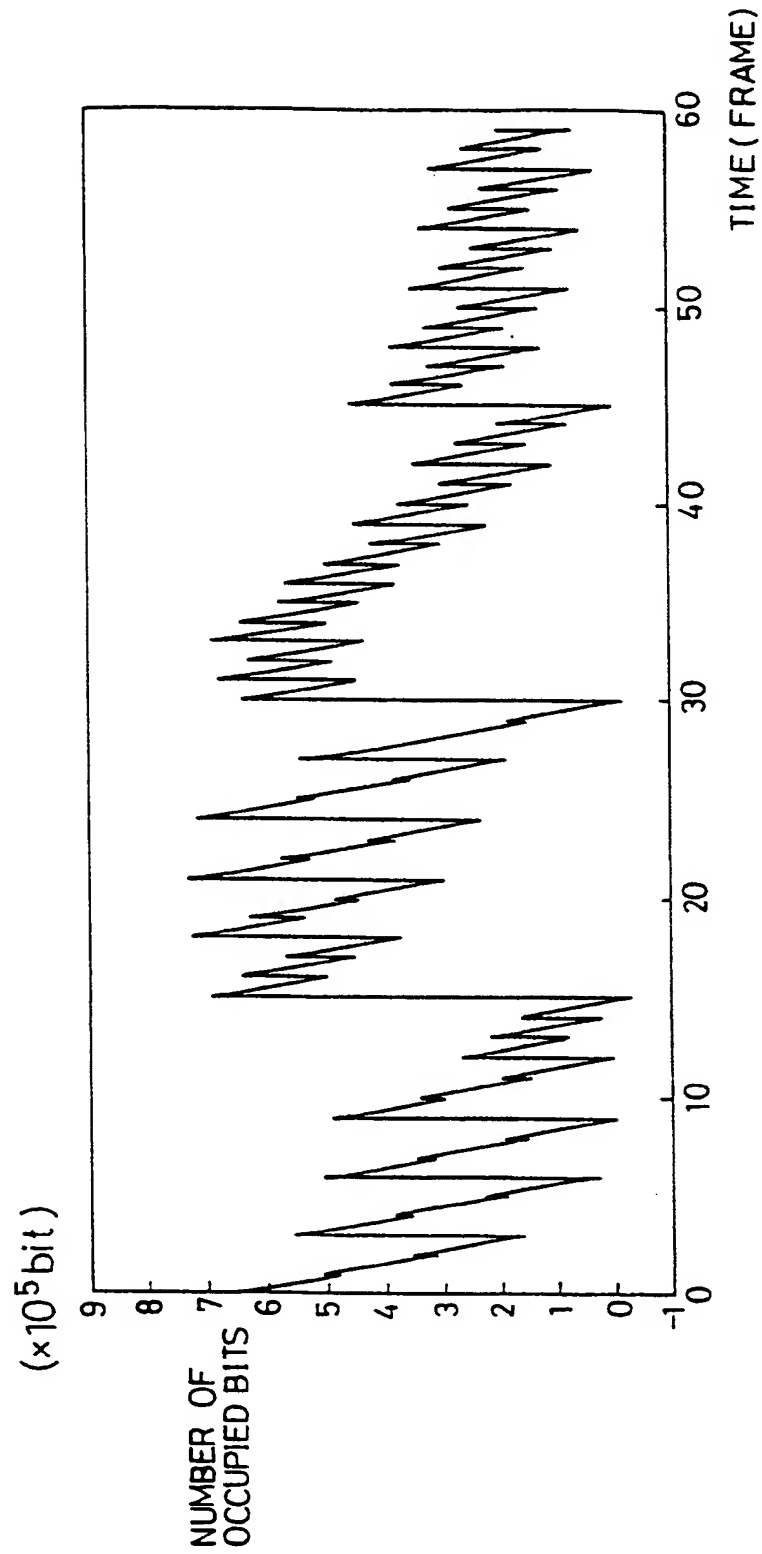


FIG. 11

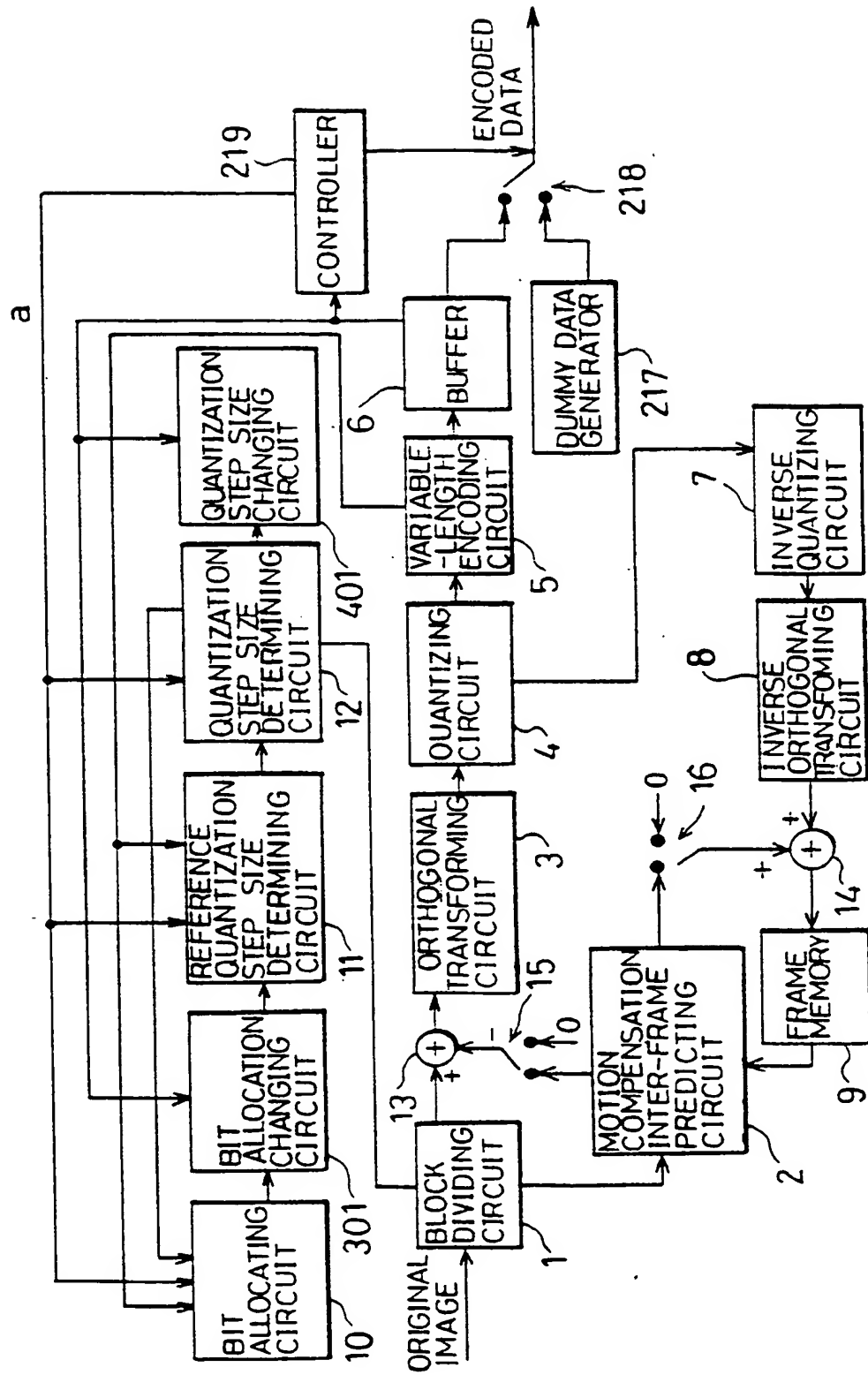


FIG. 12

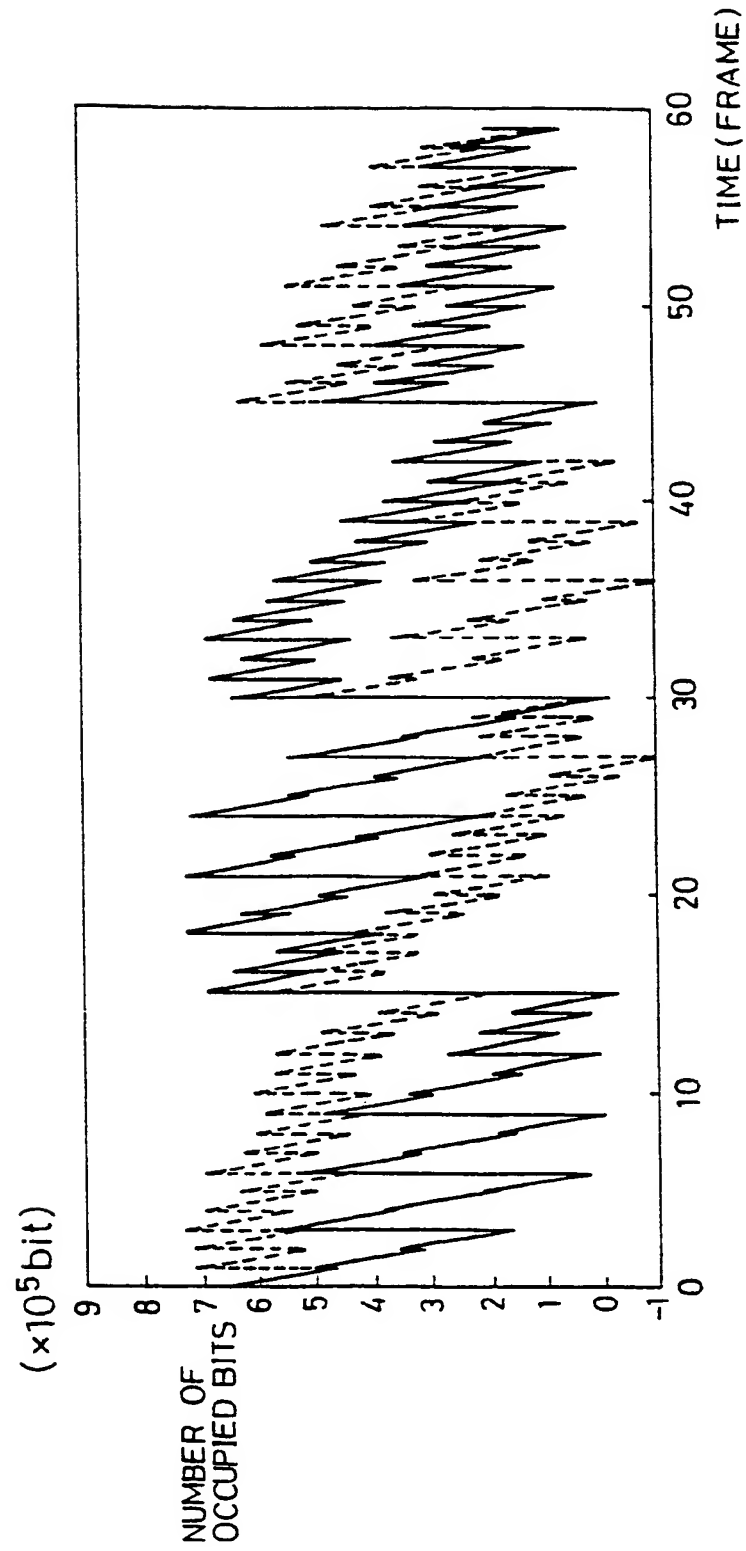


FIG. 13

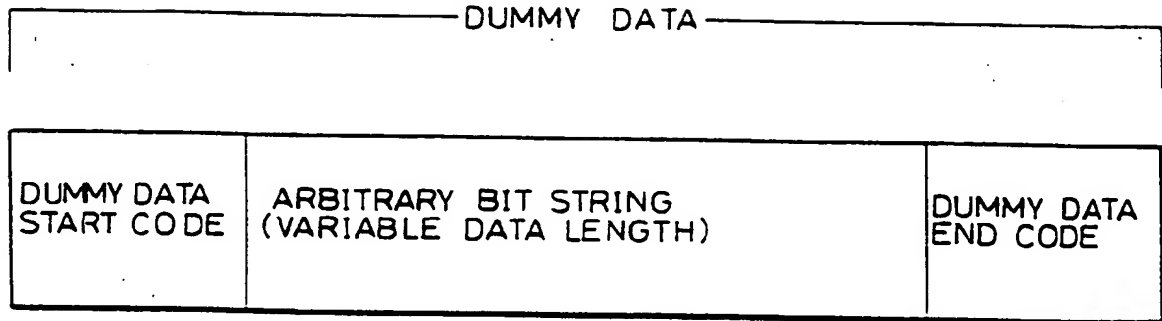


FIG. 14

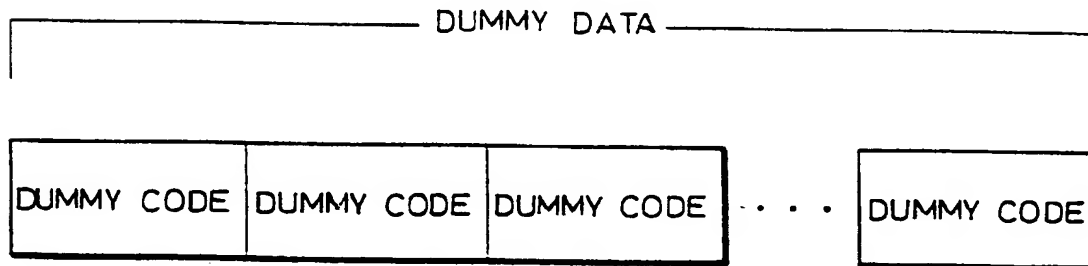


FIG. 15

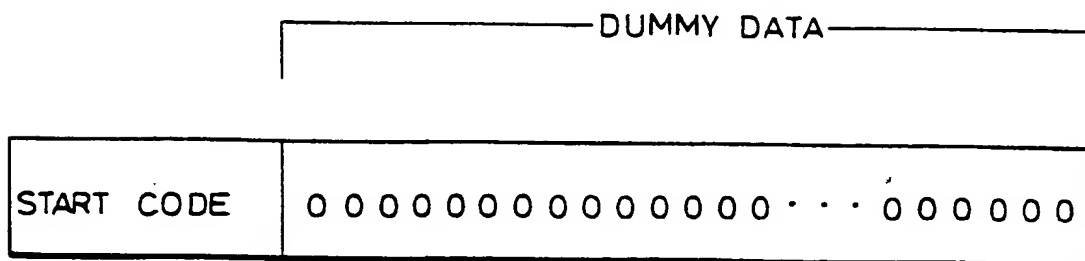


FIG. 16

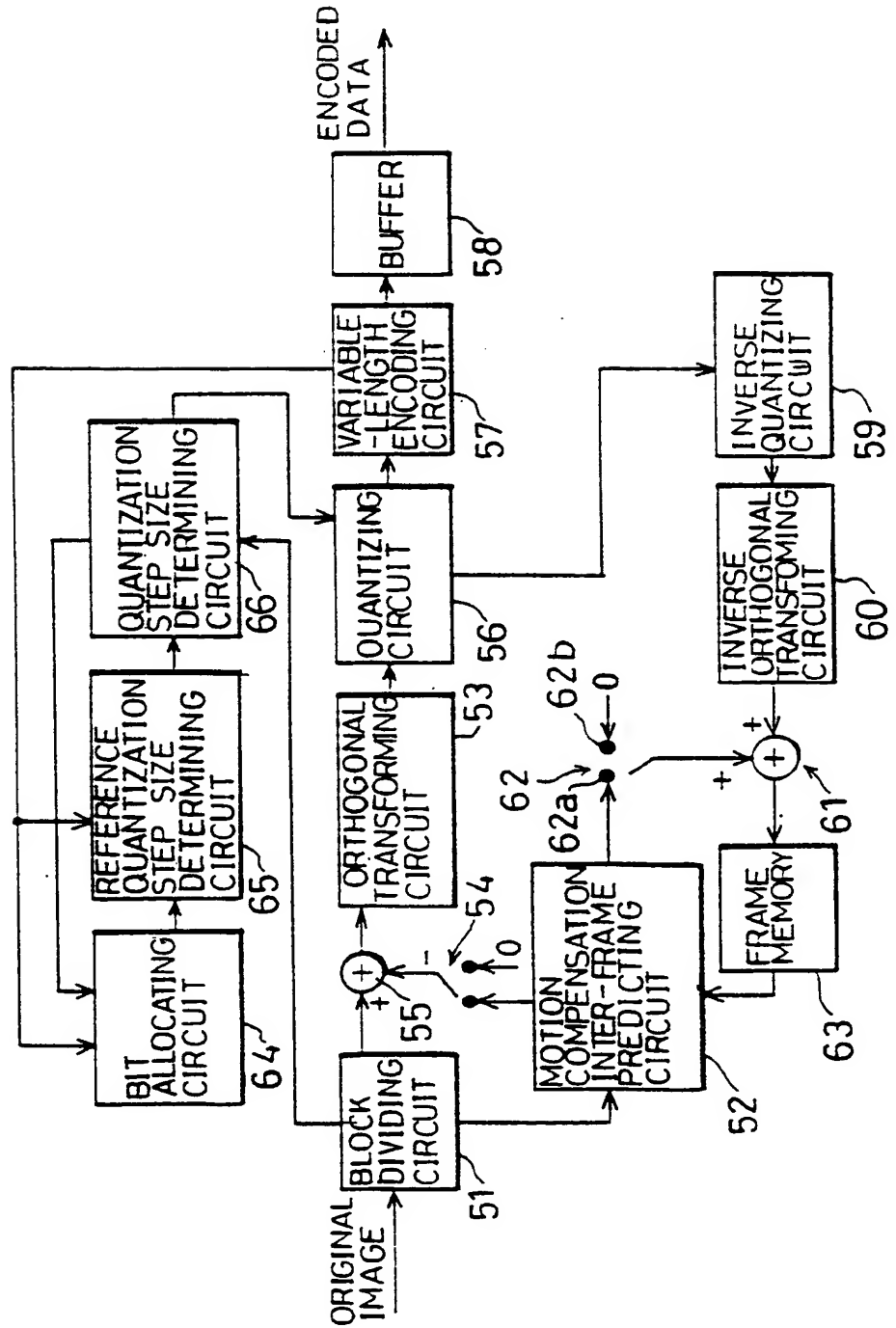


FIG. 17

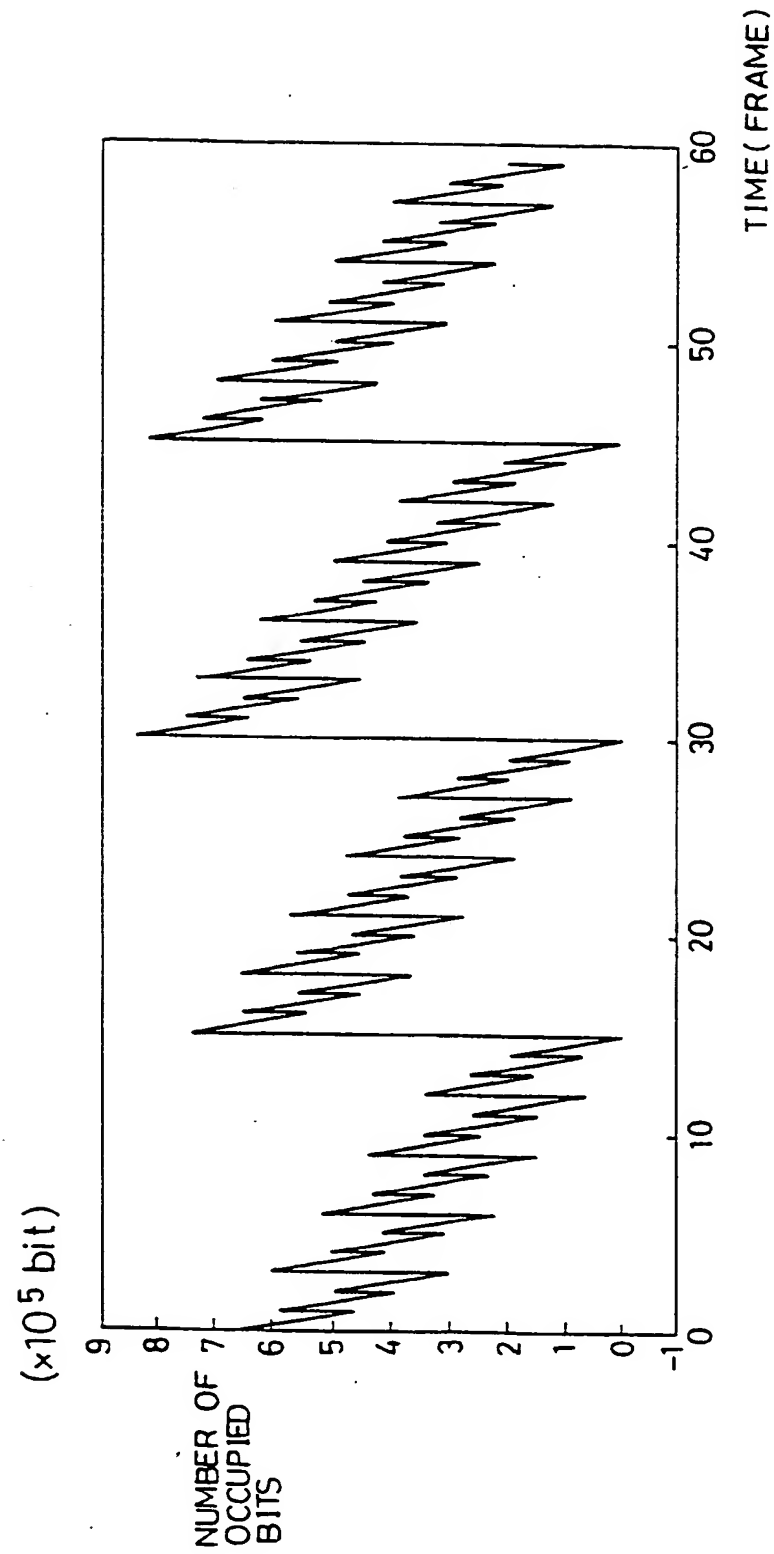
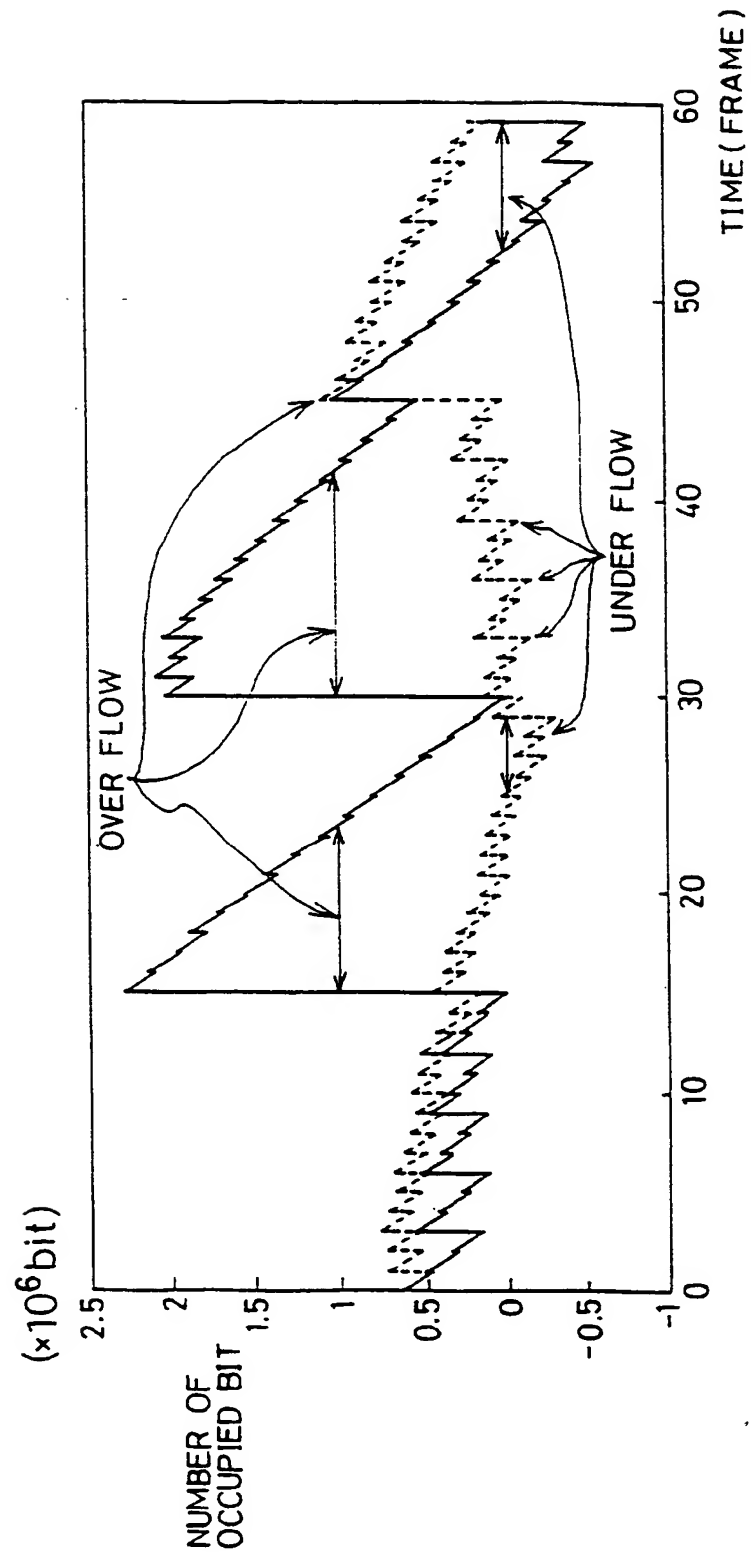


FIG. 18





(12)

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(71) Applicant: **SHARP KABUSHIKI KAISHA**
Osaka 545 (JP)

(72) Inventors:

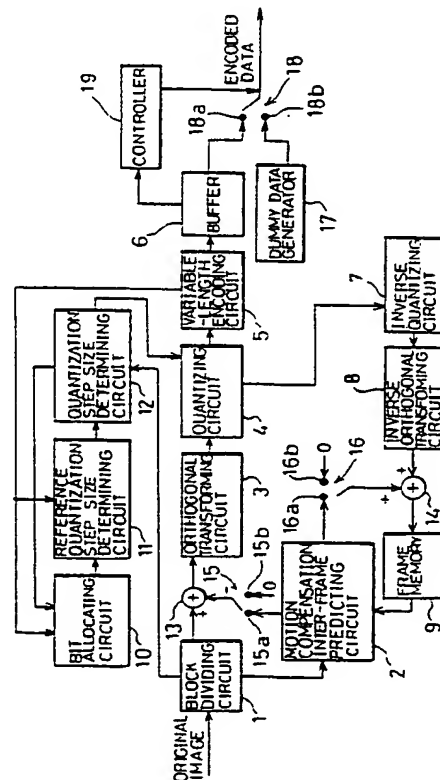
- **Katata, Hiroyuki**
Goi Ichihara-shi, Chiba 290 (JP)
- **Kusao, Hiroshi**
Chiba-shi, Chiba 267 (JP)
- **Fujiwara, Yohichi**
Chiba-shi, Chiba 266 (JP)

(74) Representative: **Brown, Kenneth Richard et al**
R.G.C. Jenkins & Co.
26 Caxton Street
London SW1H 0RJ (GB)

(54) Image encoding apparatus

(57) In an image encoding apparatus, image information is quantized and variable-length encoding is performed thereon so that the data are stored in a buffer. Thereafter, the data in the buffer are transmitted to the outside at a fixed data rate. At this time, a controller monitors a number of occupied bits in the buffer, and when the number of occupied bits is not more than thresholds, the controller switches the output of the apparatus to a dummy data generator. At this time, a parameter which is used for rate control is initialized, and dummy data which can be eliminated on a decoding circuit are outputted from the dummy data generator. Furthermore, bit allocation is changed so that a sum of the number of occupied bits and the bit allocation to a frame which is determined before encoding does not exceed a fixed amount. Moreover, when the number of occupied bits exceeds the fixed value, a quantization step size is changed to a greater value.

FIG. 1





European Patent
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EUROPEAN SEARCH REPORT

Application Number
EP 94 30 9576

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.CL6)
X	US-A-5 235 618 (SAKAI ET AL) * column 7, line 42 - column 8, line 47 * * claims 4,5,7 * * figures 4,5,9 *	1,20	H04N7/24
A	---	3-8,10	
X	EP-A-0 536 630 (KABUSHIKI KAISHA TOSHIBA) * page 58, line 47 - line 48 * * claim 33 * * figure 1 *	20	
A	---	2-7	TECHNICAL FIELDS SEARCHED (Int.CL6) H04N
X	SIGNAL PROCESSING IMAGE COMMUNICATION., vol. 5, no. 1/2, February 1993 AMSTERDAM NL, pages 21-37, XP 000345611 CHEN ET AL 'Hybrid extended MPEG video coding algorithm for general video applications' * page 28, left column, paragraph 3 - page 29, right column, paragraph 1 * * figure 3 *	12,14-18	
A	---	13,19	
X	VISUAL COMMUNICATION AND IMAGE PROCESSING '91: VISUAL COMMUNICATION, vol. 1605, no. 1, 11 November 1991 BOSTEN, MA, US, pages 58-72, XP 000479218 VISCITO ET AL 'A VIDEO COMPRESSION ALGORITHM WITH ADAPTIVE BIT ALLOCATION AND QUANTIZATION' * page 62, last paragraph - page 65, paragraph 1 * * page 68, last paragraph * * page 71, paragraph 2 * * figure 2 *	12-19	
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 17 January 1996	Examiner Dippel, U
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document			

EPO FORM 1503 03.12 (PM/C01)



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CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

- ☐ All claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for all claims.
- ☐ Only part of the claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claims:
- ☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet -B-

- ☒ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.
- ☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respects of which search fees have been paid, namely claims:
- ☐ None of the further search fees has been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:



European Patent
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EUROPEAN SEARCH REPORT

Application Number
EP 94 30 9576

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
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A	US-A-4 989 130 (MORIYAMA ET AL) * column 9, line 35 - line 68 * * column 11, line 26 - line 37 * * figure 4 5 6B 9 *	1,2,8-11	
P,A A	US-A-5 319 457 (NAKASHASHI ET AL) 7 June 1994 & JP-A-05 068 243 (HITACHI LTD) 19 March 1993 * column 4, line 15 - line 29 * * column 5, line 1 - line 7 *	1,3-7 1,3-7	
A	US-A-5 163 056 (HAGIWARA ET AL) * figures *	2,8-11	
A	EP-A-0 493 136 (VICTOR COMPANY OF JAPAN LTD) * column 5, line 44 - column 6, line 36 * * figure 1 * * column 10, line 29 - column 11, line 16 * * claims 1,2 *	12,13, 15-19	
A	US-A-5 038 209 (HANG) * column 4, line 3 - line 34 * * claims 6-8,12,13 * * figure 3 *	13,19	
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 17 January 1996	Examiner Dippel, U
<p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document</p>			

EPO FORM 1501 01.82 (P04 COI)



European Patent
Office

EP 94 30 9576 -B-

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirement of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims 1-11,20: In order to avoid underflow of the buffer used to adopt a variable data rate to a channel with fixed data rate, the encoder is completely disconnected from the channel, instead, dummy data are sent to the channel with the data rate required by the channel
2. Claims 12-19 : In order to avoid the overflow of the said buffer, the quantization step size is changed in order to generate a smaller amount of data

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